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# DM74LS109A Dual Positive-Edge-Triggered J-K Flip-Flop with Preset, Clear, and Complementary Outputs

## **General Description**

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This device contains two independent positive-edge-triggered J-K flip-flops with complementary outputs. The J and K data is accepted by the flip-flop on the rising edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the J and K inputs may be changed while the clock is HIGH or LOW as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

# **Ordering Code:**

| Order Number           | Package Number           | Package Description   |
|------------------------|--------------------------|---|
| DM74LS109AM            |                          | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| DM74LS109AN            | N16E                     | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide       |
| Devices also available | in Tape and Reel Specify | y by appending the suffix letter "X" to the ordering code                   |

## **Connection Diagram**



#### **Function Table**

|    | I   | nputs      | Outputs |   |                |                  |  |
|----|-----|------------|---------|---|----------------|------------------|--|
| PR | CLR | CLK        | J       | ĸ | Q              | Q                |  |
| L  | Н   | Х          | Х       | Х | Н              | L                |  |
| н  | L   | х          | Х       | Х | L              | н                |  |
| L  | L   | х          | Х       | Х | H (Note 1)     | H (Note 1)       |  |
| н  | н   | Ŷ          | L       | L | L              | н                |  |
| н  | н   | $\uparrow$ | н       | L | Toggle         |                  |  |
| н  | н   | $\uparrow$ | L       | н | Q <sub>0</sub> | $\overline{Q}_0$ |  |
| н  | Н   | Ŷ          | н       | н | н              | L                |  |
| н  | н   | L          | х       | х | Q <sub>0</sub> | $\overline{Q}_0$ |  |

H = HIGH Logic Leve L = LOW Logic Level

X = Either LOW or HIGH Logic Level

↑ = Rising Edge of Pulse

 $\mathsf{Q}_0=\mathsf{The}$  output logic level of  $\mathsf{Q}$  before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each active transition of the clock pulse.

Note 1: This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (HIGH) state.

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# Absolute Maximum Ratings(Note 2)

| Supply Voltage                       | 7V                                |
|--------------------------------------|-----------------------------------|
| Input Voltage                        | 7V                                |
| Operating Free Air Temperature Range | $0^{\circ}C$ to $+70^{\circ}C$    |
| Storage Temperature Range            | $-65^{\circ}C$ to $+150^{\circ}C$ |

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

# **Recommended Operating Conditions**

| Symbol           | Parame                         | Min        | Nom | Max  | Units |     |
|------------------|--------------------------------|------------|-----|------|-------|-----|
| V <sub>CC</sub>  | Supply Voltage                 | 4.75       | 5   | 5.25 | V     |     |
| VIH              | HIGH Level Input Voltag        | е          | 2   |      |       | V   |
| V <sub>IL</sub>  | LOW Level Input Voltage        | 9          |     |      | 0.8   | V   |
| I <sub>ОН</sub>  | HIGH Level Output Curr         | ent        |     |      | -0.4  | mA  |
| I <sub>OL</sub>  | LOW Level Output Curre         | ent        |     |      | 8     | mA  |
| f <sub>CLK</sub> | Clock Frequency (Note 3)       |            | 0   |      | 25    | MHz |
| f <sub>CLK</sub> | Clock Frequency (Note 4)       |            | 0   |      | 20    | MHz |
| t <sub>W</sub>   | Pulse Width                    | Clock HIGH | 18  |      |       |     |
|                  | (Note 3)                       | Preset LOW | 15  |      |       | ns  |
|                  |                                | Clear LOW  | 15  |      |       |     |
| t <sub>W</sub>   | Pulse Width                    | Clock HIGH | 25  |      |       | ns  |
|                  | (Note 4)                       | Preset LOW | 20  |      |       |     |
|                  |                                | Clear LOW  | 20  |      |       |     |
| t <sub>SU</sub>  | Setup Time                     | Data HIGH  | 30↑ |      |       |     |
|                  | (Note 3)(Note 5)               | Data LOW   | 20↑ |      |       | ns  |
| t <sub>SU</sub>  | Setup Time                     | Data HIGH  | 35↑ |      |       |     |
|                  | (Note 5)(Note 4) Data LOW      |            | 25↑ |      |       | ns  |
| t <sub>H</sub>   | Hold Time (Note 6)             |            | 0↑  |      |       | ns  |
| T <sub>A</sub>   | Free Air Operating Temperature |            | 0   |      | 70    | °C  |

**Note 3:**  $C_L = 15 \text{ pF}$ ,  $R_L = 2 \text{ k}\Omega$ ,  $T_A = 25^{\circ}\text{C}$  and  $V_{CC} = 5\text{V}$ .

Note 4:  $C_L = 50 \text{ pF}$ ,  $R_L = 2 \text{ k}\Omega$ ,  $T_A = 25^{\circ}\text{C}$  and  $V_{CC} = 5\text{V}$ .

Note 5: The symbol (  $\uparrow$  ) indicates the rising edge of the clock pulse is used for reference.

Note 6:  $T_A$  = 25°C and  $V_{CC}$  = 5V.

| Symbol                                      | Parameter                    | Condition  | าร     | Min  | Typ<br>(Note 7) | Max  | Units |
|---|------------------------------|--|--------|------|-----------------|------|-------|
| VI  | Input Clamp Voltage          | $V_{CC} = Min, I_I = -18 mA$                                 |        |      |                 | -1.5 | V     |
| V <sub>OH</sub>                             | HIGH Level<br>Output Voltage | $V_{CC} = Min, I_{OH} = Max$<br>$V_{IL} = Max, V_{IH} = Min$ | 2.7    | 3.4  |                 | V    |       |
| V <sub>OL</sub> LOW Level<br>Output Voltage |                              | $V_{CC} = Min, I_{OL} = Max$<br>$V_{IL} = Max, V_{IH} = Min$ |        |      | 0.35            | 0.5  | V     |
|   |                              | $I_{OL} = 4 \text{ mA}, V_{CC} = \text{Min}$                 |        | 0.25 | 0.4             | ĺ    |       |
| l <sub>l</sub>                              | Input Current @ Max          | V <sub>CC</sub> = Max  | J, K   |      |                 | 0.1  |       |
|   | Input Voltage                | $V_{I} = 7V$   | Clock  |      |                 | 0.1  | mA    |
|   |                              |  | Preset |      |                 | 0.2  |       |
|   |                              |  | Clear  |      |                 | 0.2  |       |
| I <sub>IH</sub>                             | HIGH Level                   | V <sub>CC</sub> = Max  | J,K    |      |                 | 20   |       |
|   | Input Current                | $V_{I} = 2.7V$   | Clock  |      |                 | 20   | μA    |
|   |                              |  | Preset |      |                 | 40   | μΛ    |
|   |                              |  | Clear  |      |                 | 40   |       |
| I <sub>IL</sub>                             | LOW Level                    | V <sub>CC</sub> = Max  | J, K   |      |                 | -0.4 |       |
|   | Input Current                | $V_I = 0.4V$   | Clock  |      |                 | -0.4 | mA    |
|   |                              |  | Preset |      |                 | -0.8 | IIIA  |
|   |                              |  | Clear  |      |                 | -0.8 |       |
| I <sub>OS</sub>                             | Short Circuit Output Current | V <sub>CC</sub> = Max (Note 8)                               |        | -20  |                 | -100 | mA    |
| Icc   | Supply Current               | V <sub>CC</sub> = Max (Note 9)                               |        |      | 4               | 8    | mA    |

Note 7: All typicals are at  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$ .

Note 8: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where  $V_0 = 2.125V$  with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 9:  $I_{CC}$  is measured with all outputs OPEN, with CLOCK grounded after setting the Q and  $\overline{Q}$  outputs HIGH in turn.

# **Switching Characteristics**

at  $V_{CC} = 5V$  and  $T_A = 25^{\circ}C$ 

| Symbol           | Parameter  | From (Input)       |                        |     |                        |     |       |
|------------------|--|--------------------|------------------------|-----|------------------------|-----|-------|
|                  |  | To (Output)        | C <sub>L</sub> = 15 pF |     | C <sub>L</sub> = 50 pF |     | Units |
|                  |  |                    | Min                    | Max | Min                    | Max | 1     |
| f <sub>MAX</sub> | Maximum Clock Frequency                            |                    | 25                     |     | 20                     |     | MHz   |
| t <sub>PLH</sub> | Propagation Delay Time<br>LOW-to-HIGH Level Output | Clock to<br>Q or Q |                        | 25  |                        | 35  | ns    |
| t <sub>PHL</sub> | Propagation Delay Time<br>HIGH-to-LOW Level Output | Clock to<br>Q or Q |                        | 30  |                        | 35  | ns    |
| t <sub>PLH</sub> | Propagation Delay Time<br>LOW-to-HIGH Level Output | Clear<br>to Q      |                        | 25  |                        | 35  | ns    |
| t <sub>PHL</sub> | Propagation Delay Time<br>HIGH-to-LOW Level Output | Clear<br>to Q      |                        | 30  |                        | 35  | ns    |
| t <sub>PLH</sub> | Propagation Delay Time<br>LOW-to-HIGH Level Output | Preset<br>to Q     |                        | 25  |                        | 35  | ns    |
| t <sub>PHL</sub> | Propagation Delay Time<br>HIGH-to-LOW Level Output | Preset<br>to Q     |                        | 30  |                        | 35  | ns    |

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