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*Dual Full-Bridge PWM Motor Driver with Brake*

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## Pre-End-of-Life

This device is in production, however, it has been deemed Pre-End of Life. The product is approaching end of life. Within a minimum of 6 months, the device will enter its final, Last Time Buy, order phase.

Date of status change: December 5, 2018

### **Recommended Substitutions:**

*For existing customer transition, and for new customers or new applications, contact Allegro Sales.*

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NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

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## Description (continued)

of a bridge, the braking function is enabled. In brake mode, both source drivers are turned off and both sink drivers are turned on, thereby dynamically braking the motor. When a logic high is applied to both INPUTs of a bridge, all output drivers are disabled.

Special power-up sequencing is not required. Internal circuit protection includes thermal shutdown with hysteresis, ground-clamp

and flyback diodes, and crossover-current protection.

The A3968 is supplied in a 16-lead plastic SOIC with two pins internally fused to the die pad for enhanced thermal dissipation. These pins are at ground potential and need no electrical isolation. The device is lead (Pb) free, with 100% matte tin leadframe plating.

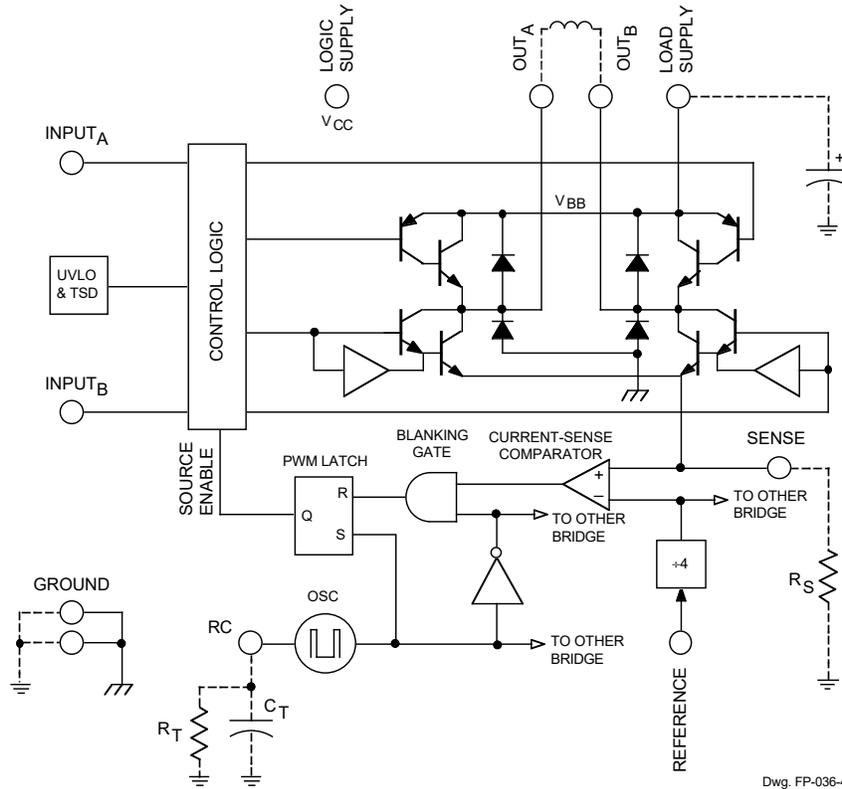
## Selection Guide

Part Number	Packing	Ambient Temperature Range (°C)
A3968SLBTR-T	1000 pieces / reel	-20 to 85

## Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units	
Load Supply Voltage	$V_{BB}$		30	V	
Logic Supply Voltage	$V_{CC}$		7.0	V	
Input Voltage	$V_{IN}$		-0.3 to $V_{CC} + 0.3$	V	
Sense Voltage	$V_S$		1.0	V	
Output Current*	$I_{OUT}$	Peak	Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or $T_J(max)$	±750	mA
		Continuous		±650	mA
Package Power Dissipation	$P_D$	$T_A = 25^\circ\text{C}$ ; per SEMI G42-88 Specification, Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance of Semiconductor Packages.	1.8	W	
Operating Ambient Temperature	$T_A$	Range E	-40 to 85	°C	
		Range S	-20 to 85	°C	
Maximum Junction Temperature	$T_J(max)$		150	°C	
Storage Temperature	$T_{stg}$		-55 to 150	°C	

**FUNCTIONAL BLOCK DIAGRAM**  
(One Half of Circuit Shown)



Dwg. FP-036-4

**TRUTH TABLE**

$INPUT_A$	$INPUT_B$	$OUT_A$	$OUT_B$	Description
L	L	L	L	Brake mode
L	H	L	H	"Forward"
H	L	H	L	"Reverse"
H	H	Z	Z	Disable

Z = High impedance

**ELECTRICAL CHARACTERISTICS** at  $T_A = +25^\circ\text{C}$ ,  $V_{BB} = 30\text{ V}$ ,  $V_{CC} = 4.75\text{ V to } 5.5\text{ V}$ ,  $V_{REF} = 2\text{ V}$ ,  $V_S = 0\text{ V}$ ,  $56\text{ k}\Omega$  &  $680\text{ pF}$  RC to Ground (unless noted otherwise)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	

#### Output Drivers

Load Supply Voltage Range	$V_{BB}$	Operating, $I_{OUT} = \pm 650\text{ mA}$ , $L = 3\text{ mH}$	$V_{CC}$	—	30	V
Output Leakage Current	$I_{CEX}$	$V_{OUT} = 30\text{ V}$	—	<1.0	50	$\mu\text{A}$
		$V_{OUT} = 0\text{ V}$	—	<-1.0	-50	$\mu\text{A}$
Output Saturation Voltage	$V_{CE(SAT)}$	Source Driver, $I_{OUT} = -400\text{ mA}$	—	1.7	2.0	V
		Source Driver, $I_{OUT} = -650\text{ mA}$	—	1.8	2.1	V
		Sink Driver, $I_{OUT} = +400\text{ mA}$ , $V_S = 0.5\text{ V}$	—	0.3	0.5	V
		Sink Driver, $I_{OUT} = +650\text{ mA}$ , $V_S = 0.5\text{ V}$	—	0.7	1.3	V
Clamp Diode Forward Voltage	$V_F$	$I_F = 400\text{ mA}$	—	1.1	1.4	V
		$I_F = 650\text{ mA}$	—	1.4	1.6	V
Motor Supply Current (No Load)	$I_{BB(ON)}$	Both bridges ON (forward or reverse)	—	3.0	5.0	mA
	$I_{BB(OFF)}$	All INPUTs = $2.4\text{ V}$	—	<1.0	200	$\mu\text{A}$

#### Control Logic

Logic Supply Voltage Range	$V_{CC}$	Operating	4.75	—	5.50	V
Logic Input Voltage	$V_{IN(1)}$		2.4	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	$V_{IN} = 2.4\text{ V}$	—	<1.0	20	$\mu\text{A}$
	$I_{IN(0)}$	$V_{IN} = 0.8\text{ V}$	—	<-20	-200	$\mu\text{A}$
Reference Input Volt. Range	$V_{REF}$	Operating	0.1	—	2.0	V
Reference Input Current	$I_{REF}$		-2.5	0	1.0	$\mu\text{A}$
Reference Divider Ratio	$V_{REF}/V_{TRIP}$		3.8	4.0	4.2	—
Current-Sense Comparator Input Offset Voltage	$V_{IO}$	$V_{REF} = 0.1\text{ V}$	-6.0	0	6.0	mV
Current-Sense Comparator Input Voltage Range	$V_S$	Operating	-0.3	—	1.0	V
Sense-Current Offset	$I_{SO}$	$I_S - I_{OUT}$ , $50\text{ mA} \leq I_{OUT} \leq 650\text{ mA}$	12	18	24	mA

NOTES: 1. Typical Data is for design information only.

2. Negative current is defined as coming out of (sourcing) the specified device terminal.

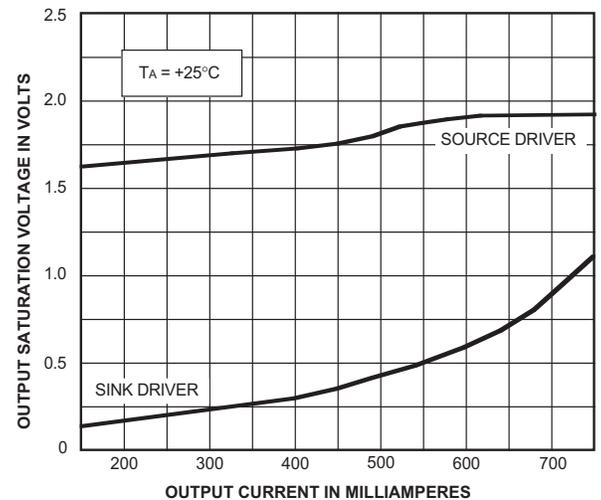
**ELECTRICAL CHARACTERISTICS at  $T_A = +25^\circ\text{C}$ ,  $V_{BB} = 30\text{ V}$ ,  $V_{CC} = 4.75\text{ V to } 5.5\text{ V}$ ,  $V_{REF} = 2\text{ V}$ ,  $V_S = 0\text{ V}$ ,  $56\text{ k}\Omega$  &  $680\text{ pF}$  RC to Ground (unless noted otherwise) (cont.)**

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
<b>Control Logic (continued)</b>						
PWM RC Frequency	$f_{osc}$	$C_T = 680\text{ pF}$ , $R_T = 56\text{ k}\Omega$	22.9	25.4	27.9	kHz
PWM Propagation Delay Time	$t_{PWM}$	Comparator Trip to Source OFF	—	1.0	1.4	$\mu\text{s}$
		Cycle Reset to Source ON	—	0.8	1.2	$\mu\text{s}$
Cross-Over Dead Time	$t_{codt}$	1 k $\Omega$ Load to 25 V	0.2	1.8	3.0	$\mu\text{s}$
Propagation Delay Times	$t_{pd}$	$I_{OUT} = \pm 650\text{ mA}$ , 50% to 90%: Disable OFF to Source ON	—	100	—	ns
		Disable ON to Source OFF	—	500	—	ns
		Disable OFF to Sink ON	—	200	—	ns
		Disable ON to Sink OFF	—	200	—	ns
		Brake Enable to Sink ON	—	2200	—	ns
		Brake Enable to Source OFF	—	200	—	ns
Thermal Shutdown Temp.	$T_J$		—	165	—	$^\circ\text{C}$
Thermal Shutdown Hysteresis	$\Delta T_J$		—	15	—	$^\circ\text{C}$
UVLO Enable Threshold	$V_{T(UVLO)+}$	Increasing $V_{CC}$	—	4.1	4.6	V
UVLO Hysteresis	$V_{T(UVLO)hys}$		0.1	0.6	—	V
Logic Supply Current	$I_{CC(ON)}$	Both bridges ON (forward or reverse)	—	—	50	mA
	$I_{CC(OFF)}$	All INPUTs = 2.4 V	—	—	9.0	mA
	$I_{CC(BRAKE)}$	All INPUTs = 0.8 V	—	—	95	mA

NOTES: 1. Typical Data is for design information only.

2. Negative current is defined as coming out of (sourcing) the specified device terminal.

Typical output saturation voltages showing Satlington sink-driver operation.



## FUNCTIONAL DESCRIPTION

**Internal PWM Current Control.** The A3968 dual full-bridges bidirectionally control two DC motors. An internal fixed-frequency PWM control circuit controls the the load current in each motor. The current-control circuitry works as follows: when the outputs of the full-bridge are turned on, current increases in the motor winding. The load current is sensed by the current-control comparator via an external sense resistor,  $R_S$ . Load current continues to increase until it reaches the predetermined value, set by the selection of external current-sensing resistors and reference input voltage ( $V_{REF}$ ) according to the equation:

$$I_{TRIP} = I_{OUT} + I_{SO} = V_{REF}/(4 R_S)$$

where  $I_{SO}$  is the sense-current error (typically 18 mA) due to the base-drive current of the sink driver transistor.

At the trip point, the comparator resets the source-enable latch, turning off the source driver of that full-bridge. The source turn-off of one full-bridge is independent of the other full-bridge. Load inductance causes the current to recirculate through the sink driver and ground-clamp diode. The current decreases until the internal clock oscillator sets the source-enable latches of both Full-bridges, turning on the source drivers of both bridges. Load current increases again, and the cycle is repeated.

The frequency of the internal clock oscillator is set by the external timing components  $R_T C_T$ . The frequency can

be approximately calculated as:

$$f_{osc} = 1/(R_T C_T + t_{blank})$$

where  $t_{blank}$  is defined below.

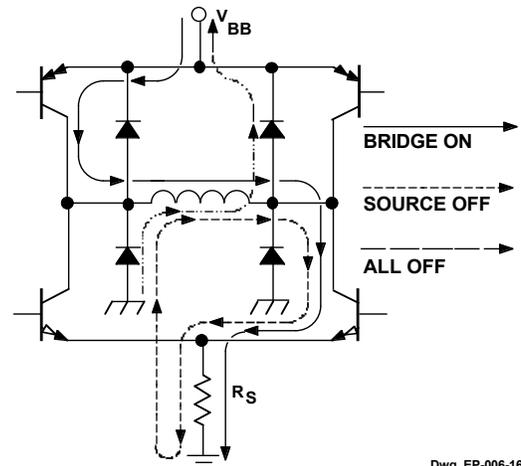
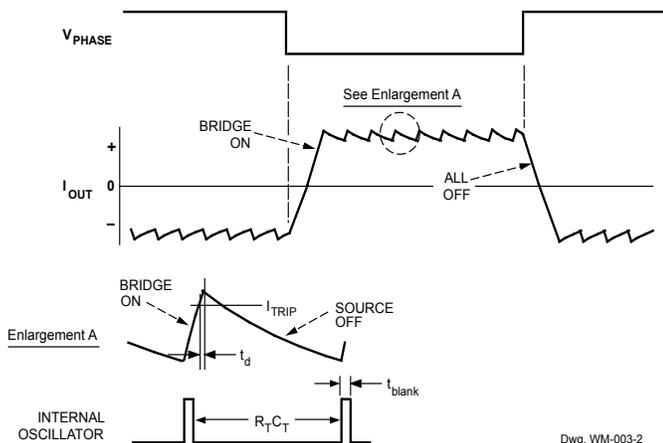
The range of recommended values for  $R_T$  and  $C_T$  are 20 to 100 k $\Omega$  and 470 to 1000 pF respectively. Nominal values of 56 k $\Omega$  and 680 pF result in a clock frequency of 25.4 kHz.

**Current-Sense Comparator Blanking.** When the source driver is turned on, a current spike occurs due to the reverse-recovery currents of the clamp diodes and switching transients related to distributed capacitance in the load. To prevent this current spike from erroneously resetting the source enable latch, the current-control comparator output is blanked for a short period of time when the source driver is turned on. The blanking time is set by the timing component  $C_T$  according to the equation:

$$t_{blank} = 1900 C_T (\mu s).$$

A nominal  $C_T$  value of 680 pF will give a blanking time of 1.3  $\mu s$ .

The current-control comparator is also blanked when the load current changes polarity (direction or phase change). This internally generated blank time is approximately 1.8  $\mu s$ .



**FUNCTIONAL DESCRIPTION** (continued)

**Load Current Regulation.** Due to internal logic and switching delays,  $t_d$ , the actual load current peak will be slightly higher than the  $I_{TRIP}$  value. These delays, plus the blanking time, limit the minimum value the current control circuitry can regulate. To produce zero current in a winding, the  $INPUT_A$  and  $INPUT_B$  terminals should be held high, turning off all output drivers for that full-bridge.

**Logic Inputs.** The direction of current in the motor winding is determined by the state of the  $INPUT_A$  and  $INPUT_B$  terminals of each bridge (see Truth Table). An internally generated dead time,  $t_{codt}$ , of approximately  $1.8 \mu s$  prevents cross-over current spikes that can occur when switching the motor direction.

A logic high on both INPUTs turns off all four output drivers of that full-bridge. This results in a fast current decay through the internal ground clamp and flyback diodes.

The appropriate  $INPUT_A$  or  $INPUT_B$  can be pulse-width modulated for applications that require a fast current-decay PWM. If external current-sensing circuitry is used, the internal current-control logic can be disabled by connecting the  $R_T C_T$  terminal to ground.

A logic low on the  $INPUT_A$  and the  $INPUT_B$  terminals will place that full-bridge in the brake mode. Both source drivers are turned off and both sink drivers are turned on. This has the effect of shorting the DC motor back-EMF voltage, resulting in a current flow that dynamically brakes the motor. Note that, during braking, the internal current-control circuitry is disabled. Therefore, care should be taken to ensure that the motor current does not exceed the absolute maximum rating of the A3968.

The REFERENCE input voltage is typically set with a resistor divider from  $V_{CC}$ . This reference voltage is internally divided down by 4 to set up the current-comparator trip-voltage threshold. The reference input voltage range is 0 to 2 V.

**Output Drivers.** To minimize on-chip power dissipation, the sink drivers incorporate a Satlington structure. The Satlington output combines the low  $V_{CE(sat)}$  features of a saturated transistor and the high peak-current capability of a Darlington (connected) transistor. A graph showing typical output saturation voltages as a function of output current is on page 5.

**Miscellaneous Information.** Thermal protection circuitry turns off all output drivers should the junction temperature reach  $165^\circ C$  typical. This is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. Normal operation is resumed when the junction temperature has decreased about  $15^\circ C$ .

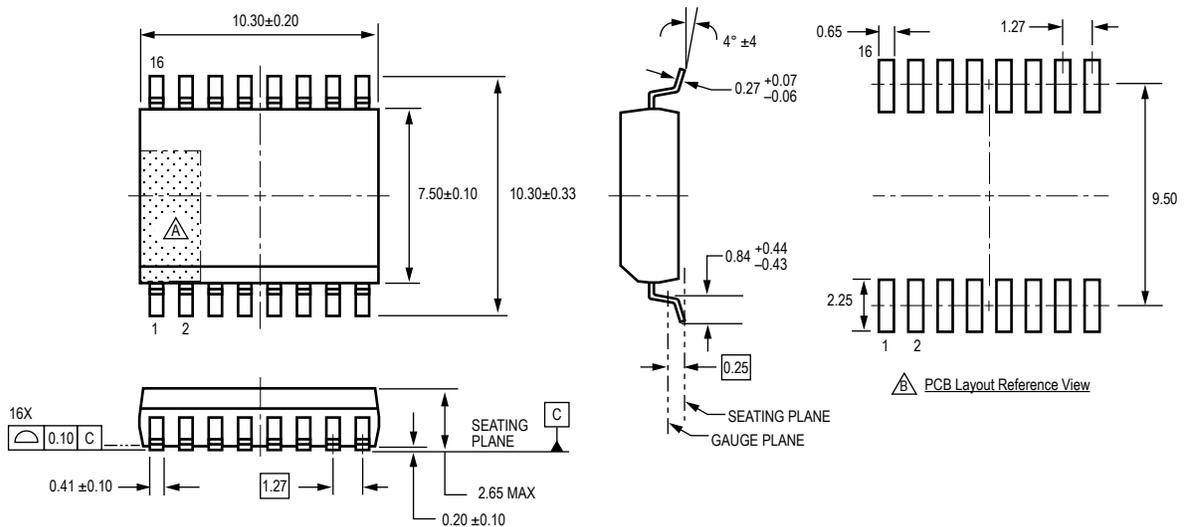
The A3968 current control employs a fixed-frequency, variable duty cycle PWM technique. As a result, the current-control regulation may become unstable if the duty cycle exceeds 50%.

To minimize current-sensing inaccuracies caused by ground trace  $I_R$  drops, each current-sensing resistor should have a separate return to the ground terminal of the device. For low-value sense resistors, the  $I \times R$  drops in the printed-wiring board can be significant and should be taken into account. The use of sockets should be avoided as their contact resistance can cause variations in the effective value of  $R_S$ .

The LOAD SUPPLY terminal,  $V_{BB}$ , should be decoupled with an electrolytic capacitor ( $47 \mu F$  recommended) placed as close to the device as physically practical. To minimize the effect of system ground  $I \times R$  drops on the logic and reference input signals, the system ground should have a low-resistance return to the load supply voltage.

The frequency of the clock oscillator will determine the amount of ripple current. A lower frequency will result in higher current ripple, but reduced heating in the motor and driver IC due to a corresponding decrease in hysteretic core losses and switching losses respectively. A higher frequency will reduce ripple current, but will increase switching losses and EMI.

Package LB, 16-pin SOICW



For Reference Only  
 Pins 4 and 13 internally fused  
 Dimensions in millimeters  
 (reference JEDEC MS-013 AA)  
 Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
 Exact case and lead configuration at supplier discretion within limits shown

**A** Terminal #1 mark area  
**B** Reference pad layout (reference IPC SOIC127P1030X265-16M)  
 All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

**Revision History**

Number	Date	Description
9	January 31, 2019	Updated product status to pre-end-of-life

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