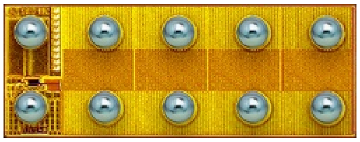
## EPC2112 – 200 V, 10 A Integrated Gate Driver eGaN® IC

### Preliminary Datasheet

**FEATURES:**

- Integrated Gate Driver
  - – Low Propagation Delay
  - – Up to 7 MHz Operation
  - – Operates from 5 V Supply
- 200 V, 40-mΩ eGaN FET
- Low Inductance 2.9 mm x 1.1 mm BGA



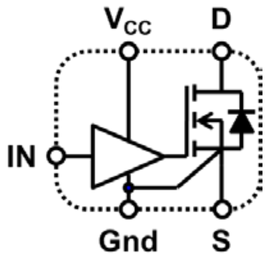
EPC2112 devices are supplied only in passivated die form with solder balls

**Die Size: 2.9 mm x 1.1 mm**

**APPLICATIONS:**

- Wireless Power (Highly Resonant and Inductive)
- High Frequency DC-DC Conversion

**Schematic Diagram**




**DESCRIPTION**

The EPC2112 enhancement-mode gallium-nitride (eGaN®) integrated driver and FET consists of a 40-mΩ, 200 V eGaN power transistor and an optimized gate driver in a low inductance 2.9 mm by 1.1 mm surface-mount BGA.

The EPC2112 monolithic IC enables designers to improve efficiency, save space, and lower costs compared to silicon-based solutions. The ultra-low capacitance and zero reverse recovery of the eGaN FET enables efficient operation in many topologies. The integrated driver is specifically matched to the GaN device to yield optimal performance under various operating conditions. Performance further enhanced due to the small, low inductance footprint. Monolithic integration eliminates interconnect inductances for higher efficiency at high frequency. This is especially important for high frequency applications such as resonant wireless power.

## ABSOLUTE MAXIMUM RATINGS

| Maximum Ratings | | | |
|---|---|---|---|
| $V_{DS}$ | Drain-to-Source Voltage (Continuous) | 200 | V |
| $I_D$ | Continuous ($T_A$ = 25˚C, $R_{\theta JA}$= 18 ˚C/W) | 10 | A |
| | Pulsed (25˚C, $T_{PULSE}$ 300 µs) | 40 | |
| $V_{IN}$ | Input Signal Voltage | 6 | V |
| $T_J$ | Operating Temperature | -40 to 150 | ˚C |
| $T_{STG}$ | Storage Temperature | -40 to 150 | |
| $V_{CC}$ | Supply Voltage | 6 | V |

## RECOMMENDED OPERATING CONDITIONS

| Recommended Operating Conditions | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | **Description** | **MIN** | **TYP** | **MAX** | **UNIT** |
| $V_{DS}$ | Drain-Source voltage | | | 160 | V |
| $V_{CC}$ | Driver Supply voltage | 4.5 | 5 | 5.5 | V |
| $I_{CC}$ | External driver supply current[1] | | | 50 | mA |
| $V_{IN,Off}$ | Input signal for turn-off | | | 0.5 | V |
| $V_{IN,On}$ | Input signal for turn-on | 4.5 | | | V |
| $V_{IN,slew}$ | Input signal slew rate | 0.25 | | | V/ns |
| $T_J$ | Operating Temperature | -40 | | 150 | °C |

[1] For up to maximum operating frequency

## THERMAL INFORMATION

| Thermal Characteristics | | | |
|---|---|---|---|
| | | **TYP** | **Unit** |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 1.7 | ˚C/W |
| $R_{\theta JB}$ | Thermal Resistance, Junction to Board | 20 | ˚C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient[2] | 66 | ˚C/W |

[2] $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

Thermal models for EPC devices available at http://epc-co.com/epc/DesignSupport/DeviceModels.aspx

## ELECTRICAL CHARACTERSTICS

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| **eGaN POWER TRANSISTOR** | | | | | | |
| $BV_{DSS}$ | Drain-to-Source Voltage | $V_{CC}$ = 0 V, $V_{IN}$ = 0 V, $I_D$ = 125 µA | 200 | | | V |
| $I_{DSS}$ | Drain -Source Leakage | $V_{DS}$ = 160 V, $T_J$ = 25 °C | | 20 | 100 | µA |
| $R_{DS(ON)}$ | Drain-Source On-Resistance | $V_{CC}$ = 5 V, $T_J$ = 25 °C | | 32 | 40 | mΩ |
| $V_{SD}$ | Source-Drain Forward Voltage | $V_{CC}$ = 5 V, $V_{IN}$ = 0 V, $I_{SD}$ = 0.5 A | | 2 | | V |
| $C_{OSS}$ | Output Capacitance | $V_{IN}$ = 0 V, $V_{CC}$ = 5 V, $V_{DS}$ = 100 V, f = 1 MHz | | 150 | | |
| $C_{OSS(ER)}$ | Energy Output Capacitance, Energy Related [3] | $V_{IN}$ = 0 V, $V_{CC}$ = 5 V, $V_{DS}$ = 0 to 100 V | | 175 | | pF |
| $C_{OSS(TR)}$ | Energy Output Capacitance, Energy Related [4] | | | 233 | | |
| $Q_{OSS}$ | Output Charge | $V_{IN}$ = 0 V, $V_{CC}$ = 5 V, $V_{DS}$ = 100 V, $V_{GS}$ = 0 V | | 24 | | nC |
| $Q_{RR}$ | Source-Drain Recovery Charge | | | 0 | | |

[3] $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 50% $BV_{DSS}$

[4] $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 50% $BV_{DSS}$

## ELECTRICAL CHARACTERSITCS

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| **DRIVER SUPPLY** | | | | | | |
| $I_{VCC, ON}$ | Quiescent current (average) | $V_{IN}$ = 5 V, $V_{CC}$ = 5 V, $V_{DS}$ = 0 V | | 4 | | |
| $I_{VCC, OFF}$ | Quiescent current (average) | $V_{IN}$ = 0 V, $V_{CC}$ = 5 V, $V_{DS}$ = 0 V | | 4 | | mA |
| $I_{VCC, OP}$ | Operating Current | 50% duty cycle, $V_{CC}$ = 5 V, $f_{SW}$ = 1 MHz | | 6.5 | | |
| $V_{IH}$ | Turn-on Input pin, logic high | $V_{CC}$ = 5 V | 4.0 | | | V |
| $V_{IL}$ | Turn-off Input pin, logic low | $V_{CC}$ = 5 V | | | 0.7 | |

## SWITCHING CHARACTERISTICS

| Switching Characteristics | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| **DRIVER[5]** | | | | | | |
| $t_{pd,on}$ | Propagation delay, turn on | $V_{CC}$ = 5 V, $V_{DS}$ = 160 V, $I_L$ = 4 A | | 2.7 | | ns |
| $t_{rise}$ | Rise Time | | | 2.7 | | ns |
| $t_{on}$ | Total turn-on time | | | 8.5 | | ns |
| $t_{pd,off}$ | Propagation delay, turn off | | | 16.9 | | ns |
| $t_{fall}$ | Fall Time | | | 5.5 | | ns |
| $t_{off}$ | Total turn-off time | | | 26.5 | | ns |
| $t_{MIN}$ | Minimum on-time | $V_{CC}$ = 5 V, $V_{BUS}$ = 160 V | | 9.2 | | ns |
| $t_{MAX}$ | Maximum on-time | $V_{CC}$ = 5 V, $I_{DS}$ = 0.5 A | | 40 | | ms |

[5] See application circuit, Figure 4 & 5

## TYPICAL CHARACTERSITCS

**Figure 1: Normalized On-State Resistance vs Temperature**

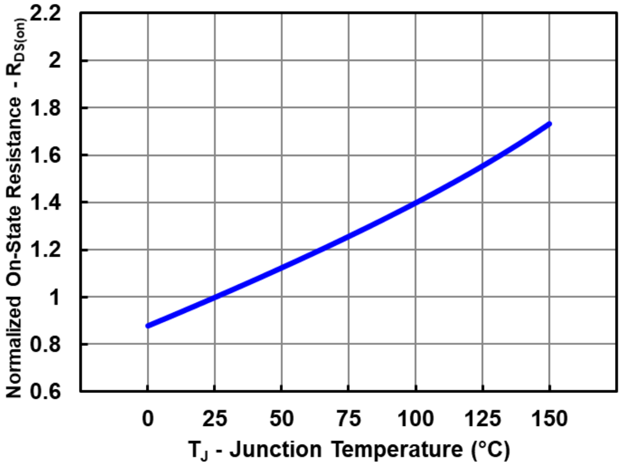



**Figure 2: Capacitance (Linear Scale)**

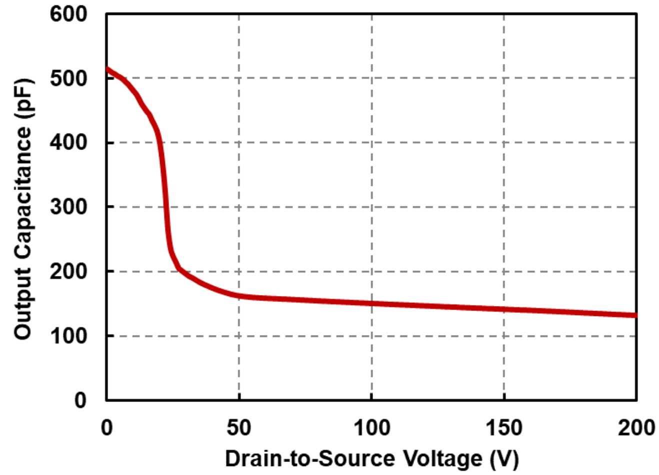



**Figure 3: Output Charge and $C_{OSS}$ Stored Energy**

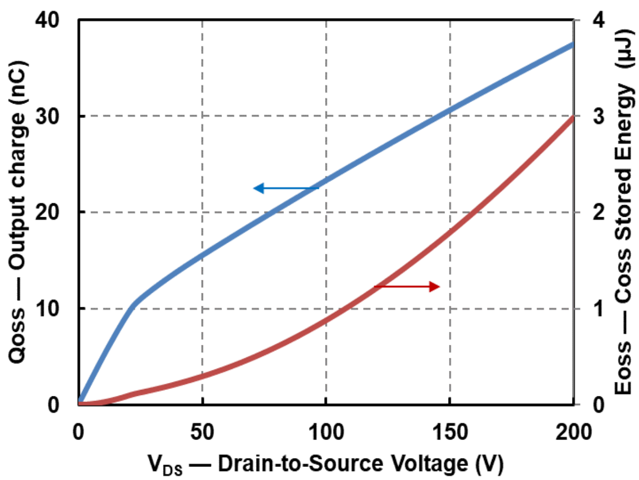


**Figure 4: Double pulse Test Definitions**

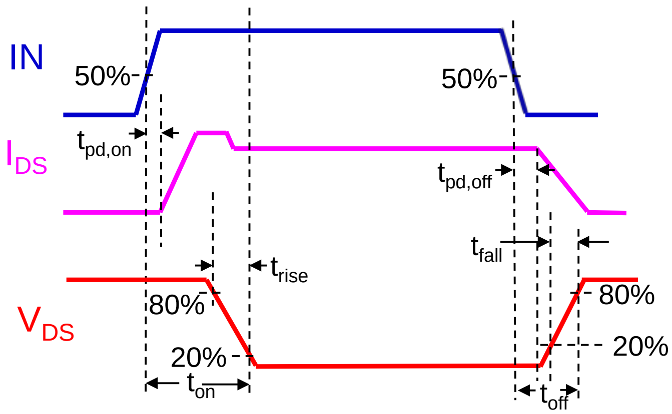
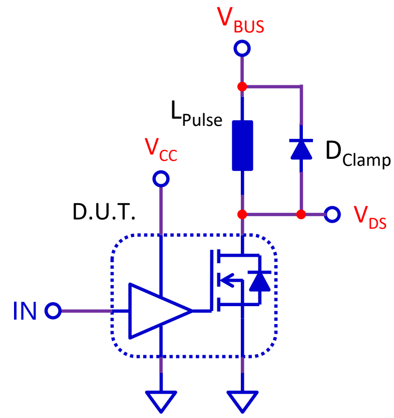
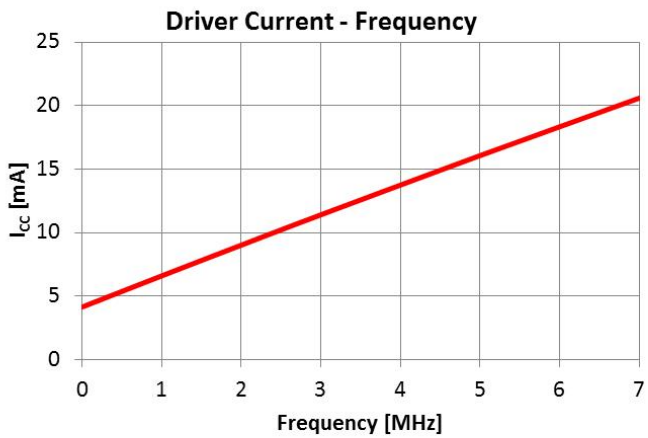



**Figure 5: Double pulse Test Circuit**



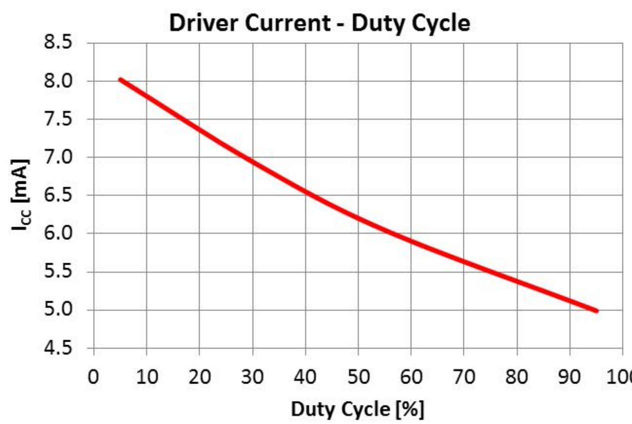

$L_{Pulse}$ = 33 µH
$D_{Clamp}$ = MBR2H200SFT3G (OnSemi)

**Figure 6: Driver quiescent current as function of frequency**



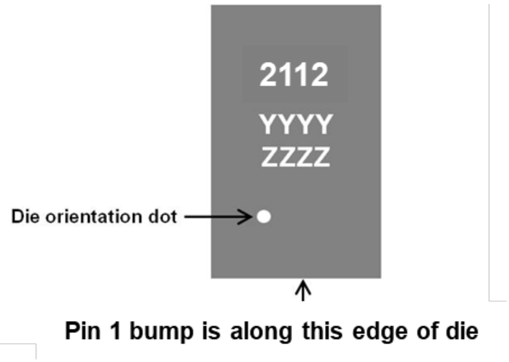

**(50% duty cycle, $V_{cc}$= 5 V, $V_{DS}$ = 0 V)**

**Figure 7: Driver quiescent current as function of duty cycle**




**(1 MHz, $V_{CC}$= 5 V, $V_{DS}$ = 0 V)**

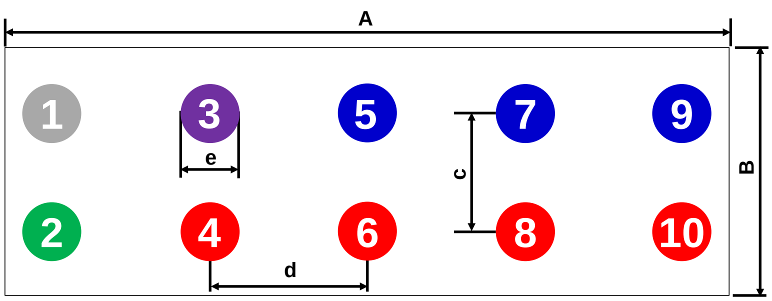
## DIE MARKINGS




| Part Number | Laser Marking | | |
|---|---|---|---|
| | Part # Marking Line 1 | Lot Date Code Marking Line 2 | Lot Date Code Marking Line 3 |
| EPC2112ENGRT | 2112 | YYYY | ZZZZ |

## DIE OUTLINE

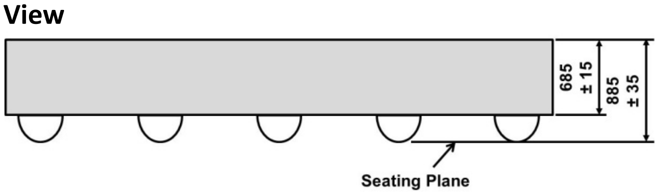
### Solder Bump View




| DIM | MICROMETERS | | |
|---|---|---|---|
| | MIN | Nominal | MAX |
| A | 2870 | 2900 | 2930 |
| B | 1070 | 1100 | 1130 |
| c | | 600 | |
| d | | 600 | |
| e | 238 | 264 | 290 |

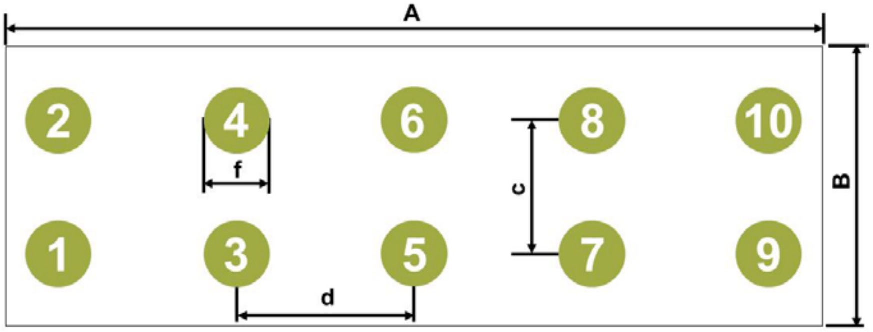
Pad 1 is Input;
Pad 2 is $V_{CC}$;
Pad 3 is Gnd;
Pads 4, 6, 8, 10 are Drain;
Pads 5, 7, 9 are Source

### Side View



## RECOMMENDED LAND PATTERN

**(*Units in µm)***



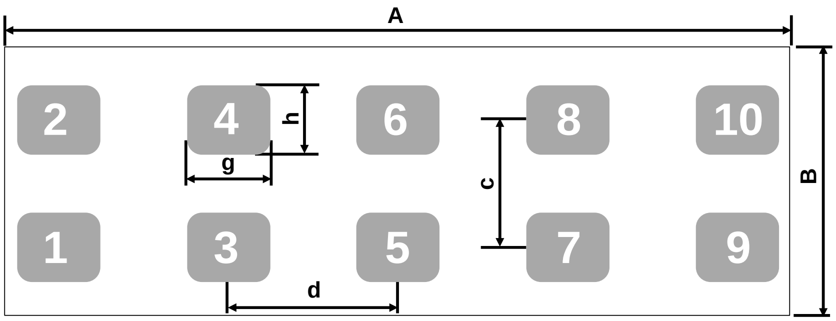

| DIM | MICROMETERS |
|---|---|
| A | 2900 |
| B | 1100 |
| c | 600 |
| d | 600 |
| f | 230 |

The land pattern is solder mask defined. Copper is larger than the solder mask opening.

## RECOMMENDED STENCIL DESIGN

**(*Units in µm)***

**Back Side View (Bump on Bottom)**




| DIM | MICROMETERS |
|---|---|
| A | 2900 |
| B | 1100 |
| c | 600 |
| d | 600 |
| g | 300 |
| h | 250 |

**Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.**

Recommended stencil should be 4mil (100µm) thick, laser cut. The corner has a radius of R60.

**Additional assembly resources available at http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx**



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