STB36NM60ND, STW36NM60ND

Automotive-grade N-channel 600 V, 0.097 Ω typ., 29 A FDmesh™ II Power MOSFETs (with fast diode) in D^2PAK and TO-247 packages

Datasheet - production data

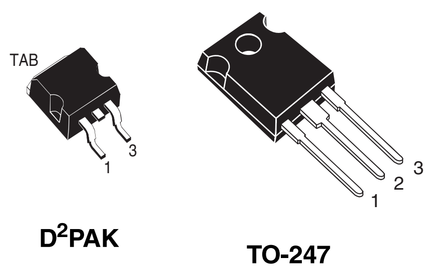
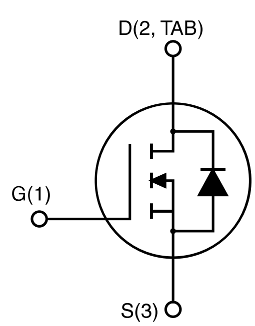


Figure 1. Internal schematic diagram



Features

Order codes	V_{DSS} @T_J max.	$R_{DS(on)}$ max.	I_D
STB36NM60ND	650 V	0.110 Ω	29 A
STW36NM60ND			

- Designed for automotive applications and AEC-Q101 qualified
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- Extremely high dv/dt and avalanche capabilities

Applications

- Automotive switching applications

Description

These FDmesh™ II Power MOSFETs with intrinsic fast-recovery body diode are produced using the second generation of MDmesh™ technology. Utilizing a new strip-layout vertical structure, these revolutionary devices feature extremely low on-resistance and superior switching performance. They are ideal for bridge topologies and ZVS phase-shift converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB36NM60ND	36NM60ND	D^2PAK	Tape and reel
STW36NM60ND	36NM60ND	TO-247	Tube

This is information on a product in full production. www.st.com

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate- source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	29	A
I_D	Drain current (continuous) at T_C = 100 °C	18	A
I_{DM} (1)	Drain current (pulsed)	116	A
P_{TOT}	Total dissipation at T_C = 25 °C	190	W
dv/dt(2)	Peak diode recovery voltage slope	40	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_J	Max. operating junction temperature	150	

1. Pulse width limited by safe operating area
2. $I_{SD} \leq$ 29 A, di/dt $\leq$ 600 A/µs, V_{DD} = 80% $V_{(BR)DSS}$,V_{DSPeak} < $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		D^2PAK	TO-247	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.66		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max		50	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb max	30		°C/W

1. When mounted on FR-4 board of 1 inch², 2 oz Cu.

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	7	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	110	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 600 V V_{DS} = 600 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 14.5 A		0.097	0.110	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	2785	-	pF
C_{oss}	Output capacitance		-	168	-	pF
C_{rss}	Reverse transfer capacitance		-	5	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 480 V	-	438	-	pF
$t_{d(on)}$	Turn-on delay time	V_{DD} =300 V, I_D = 14.5 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 16* and *21*)	-	30	-	ns
t_r	Rise time		-	53.4	-	ns
$t_{d(off)}$	Turn-off delay time		-	111	-	ns
t_f	Fall time		-	61.8	-	ns
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 29 A, V_{GS} = 10 V, *(see Figure 17)*	-	80.4	-	nC
Q_{gs}	Gate-source charge		-	16	-	nC
Q_{gd}	Gate-drain charge		-	41.4	-	nC
R_g	Gate input resistance	f=1 MHz , open drain	-	2.87	-	Ω

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		29 116	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 29 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 29 A, V_{DD} = 60 V di/dt=100 A/µs *(see Figure 18)*	-	175		ns
Q_{rr}	Reverse recovery charge		-	1.4		µC
I_{RRM}	Reverse recovery current		-	16		A
t_{rr}	Reverse recovery time	I_{SD} = 29 A,V_{DD} = 60 V di/dt=100 A/µs, T_J = 150 °C *(see Figure 18)*	-	255		ns
Q_{rr}	Reverse recovery charge		-	2.6		µC
I_{RRM}	Reverse recovery current		-	20		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D^2PAK

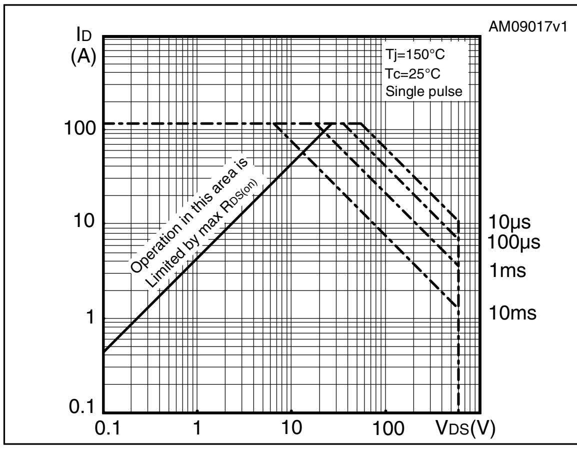


Figure 3. Thermal impedance for D^2PAK

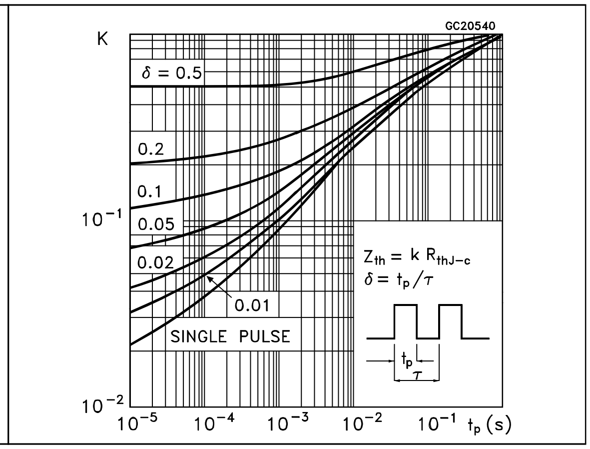


Figure 4. Safe operating area for TO-247

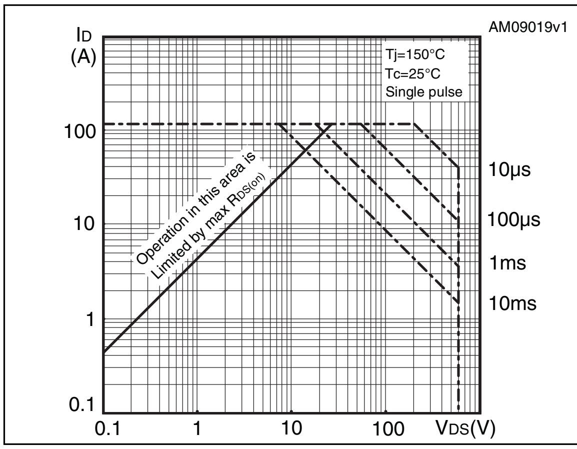


Figure 5. Thermal impedance for TO-247

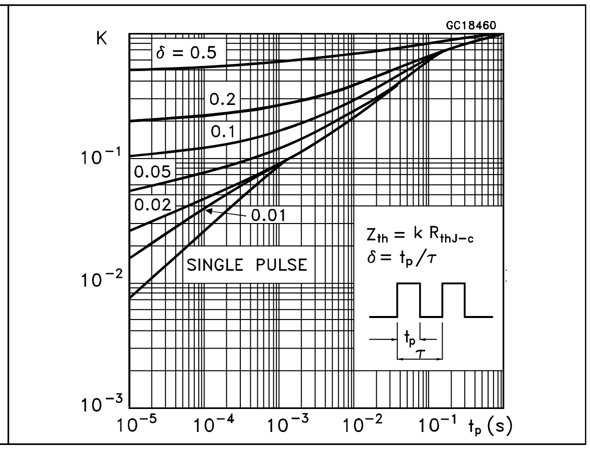


Figure 6. Output characteristics

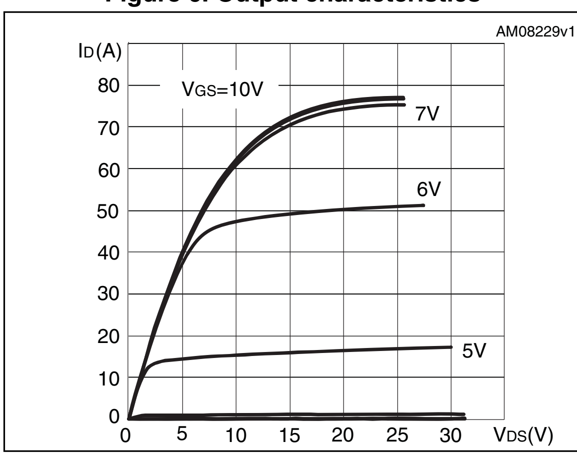


Figure 7. Transfer characteristics

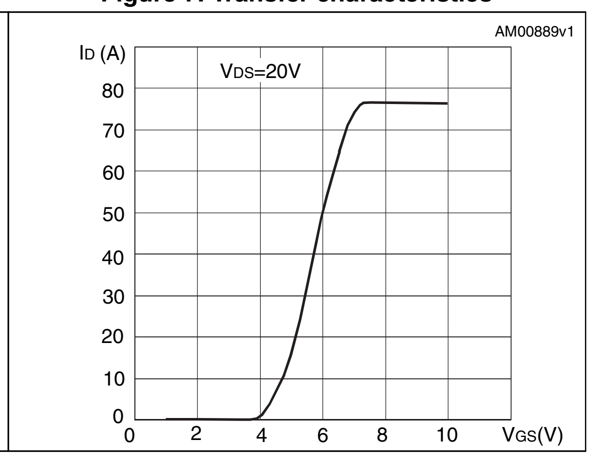


Figure 8. Gate charge vs gate-source voltage

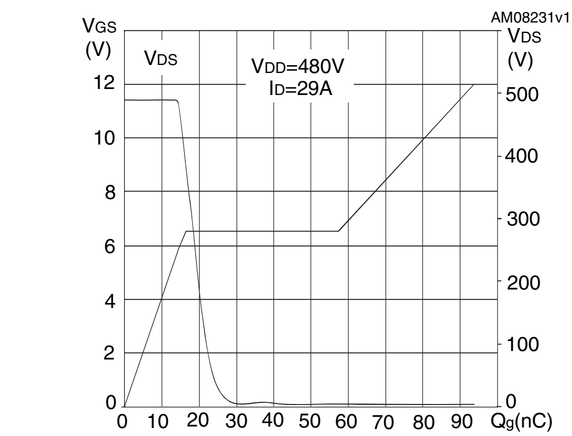


Figure 9. Static drain-source on-resistance

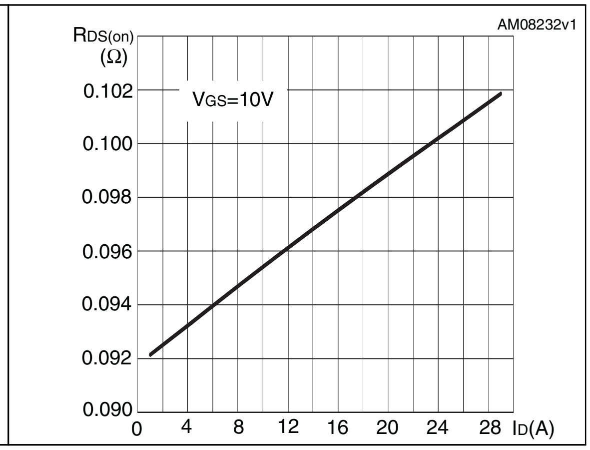


Figure 10. Capacitance variations

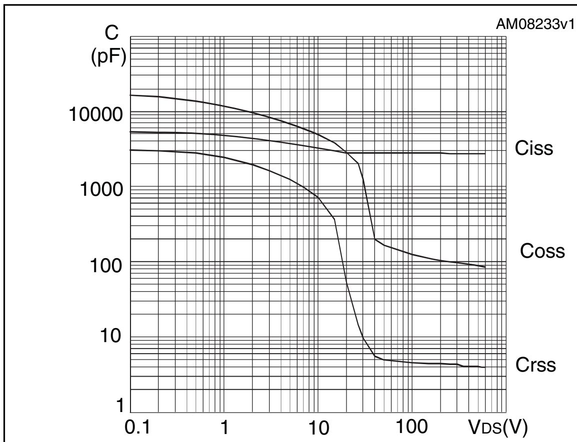


Figure 11. Output capacitance stored energy

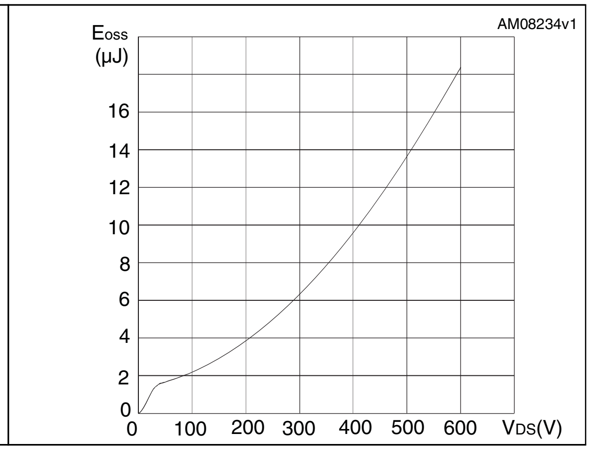


Figure 12. Normalized gate threshold voltage vs temperature

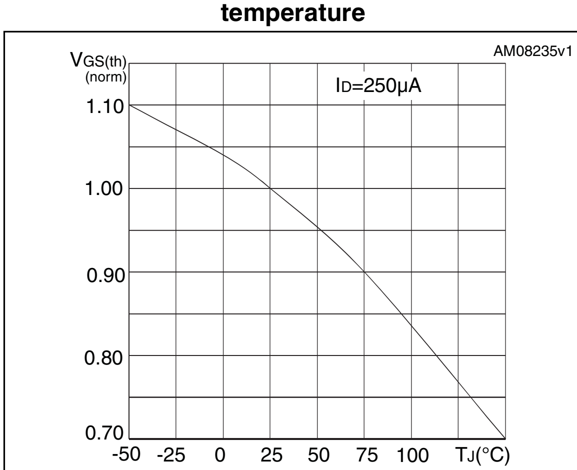


Figure 13. Normalized on-resistance vs temperature

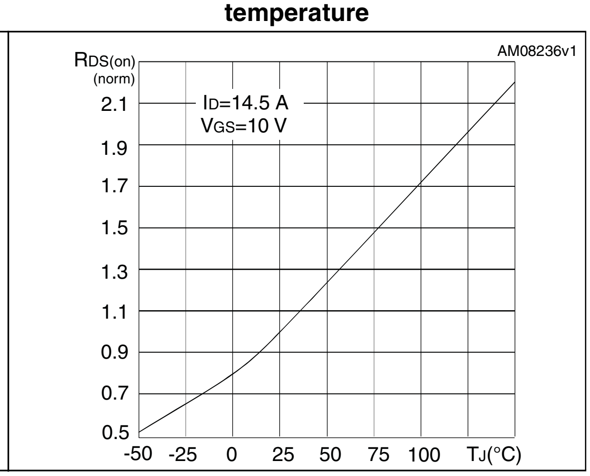


Figure 14. Normalized V_{DS} vs temperature

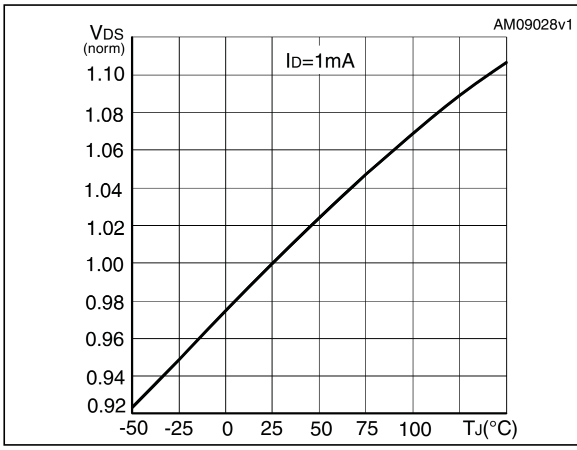
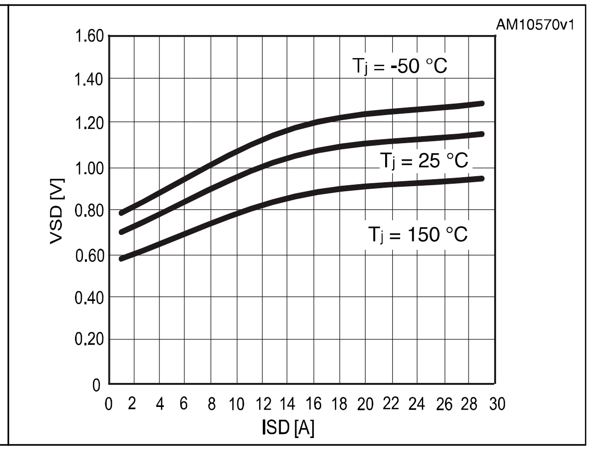


Figure 15. Source-drain diode forward vs temperature



3 Test circuits

Figure 16. Switching times test circuit for resistive load

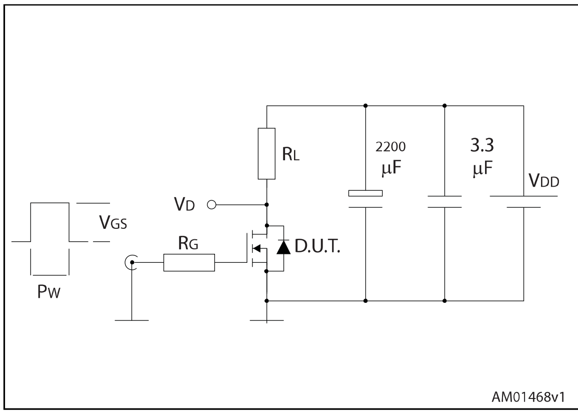


Figure 17. Gate charge test circuit

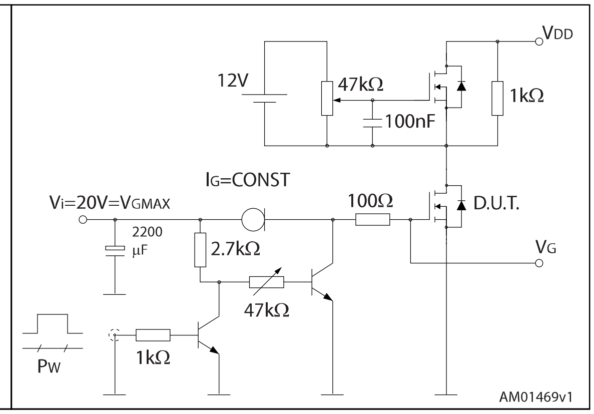


Figure 18. Test circuit for inductive load switching and diode recovery times

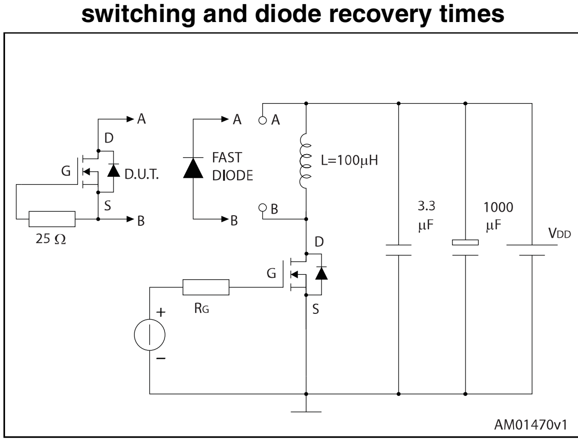


Figure 19. Unclamped inductive load test circuit

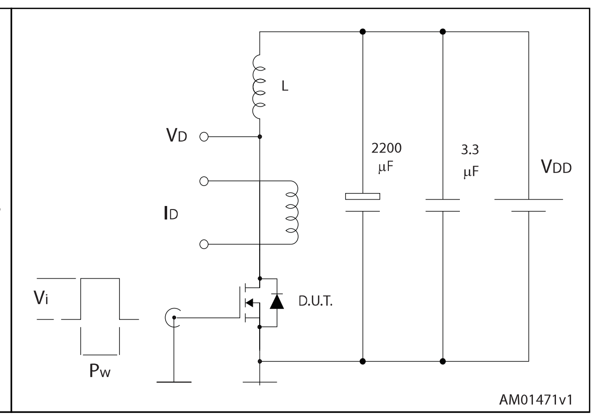


Figure 20. Unclamped inductive waveform

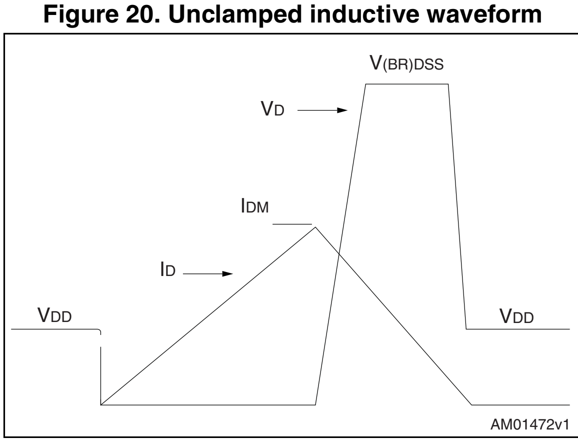
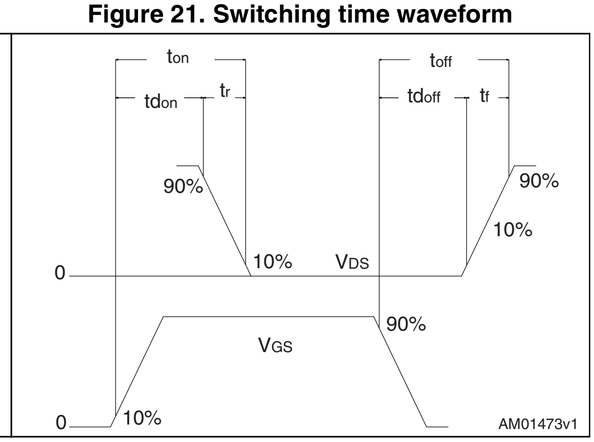


Figure 21. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 8. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 22. D²PAK (TO-263) drawing

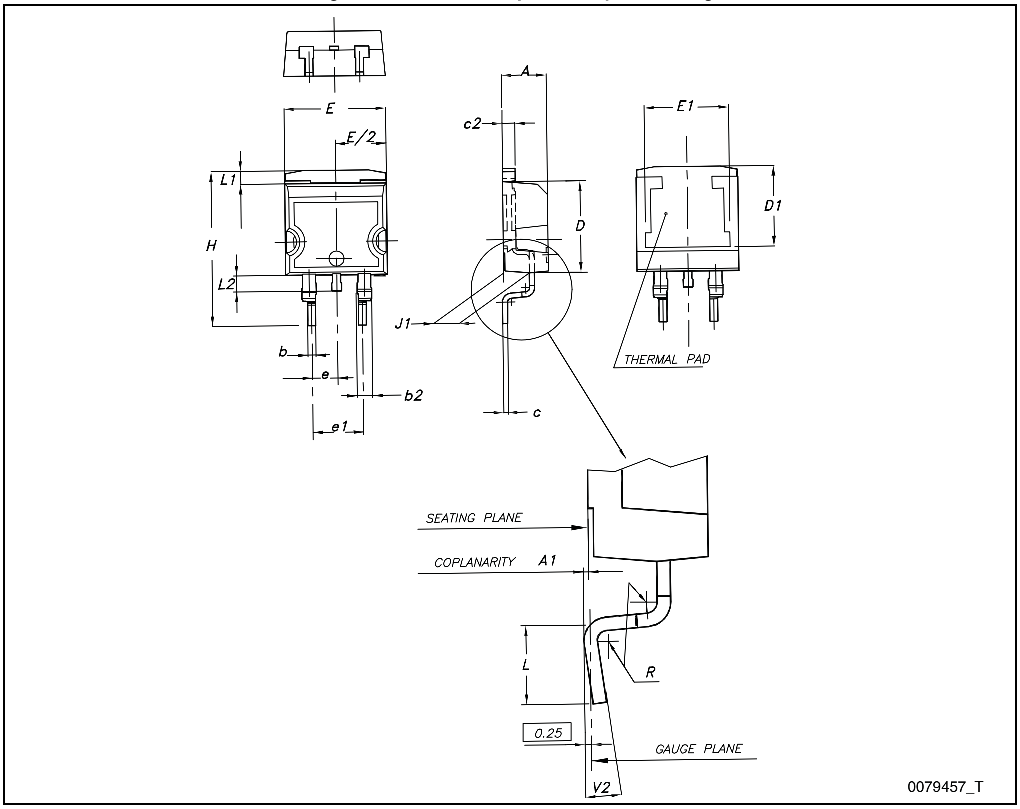
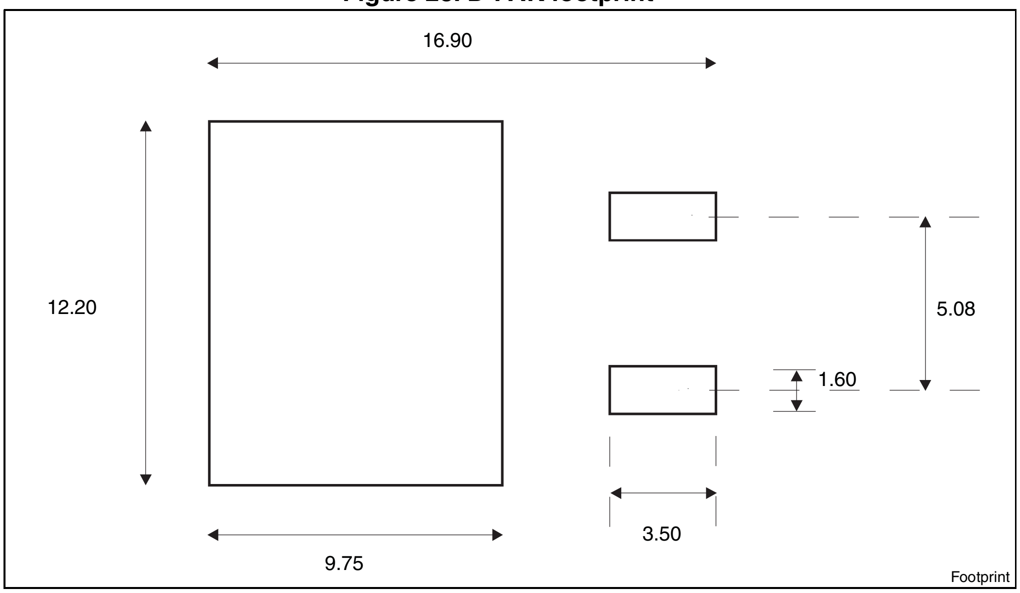


Figure 23. D²PAK footprint[(a)]

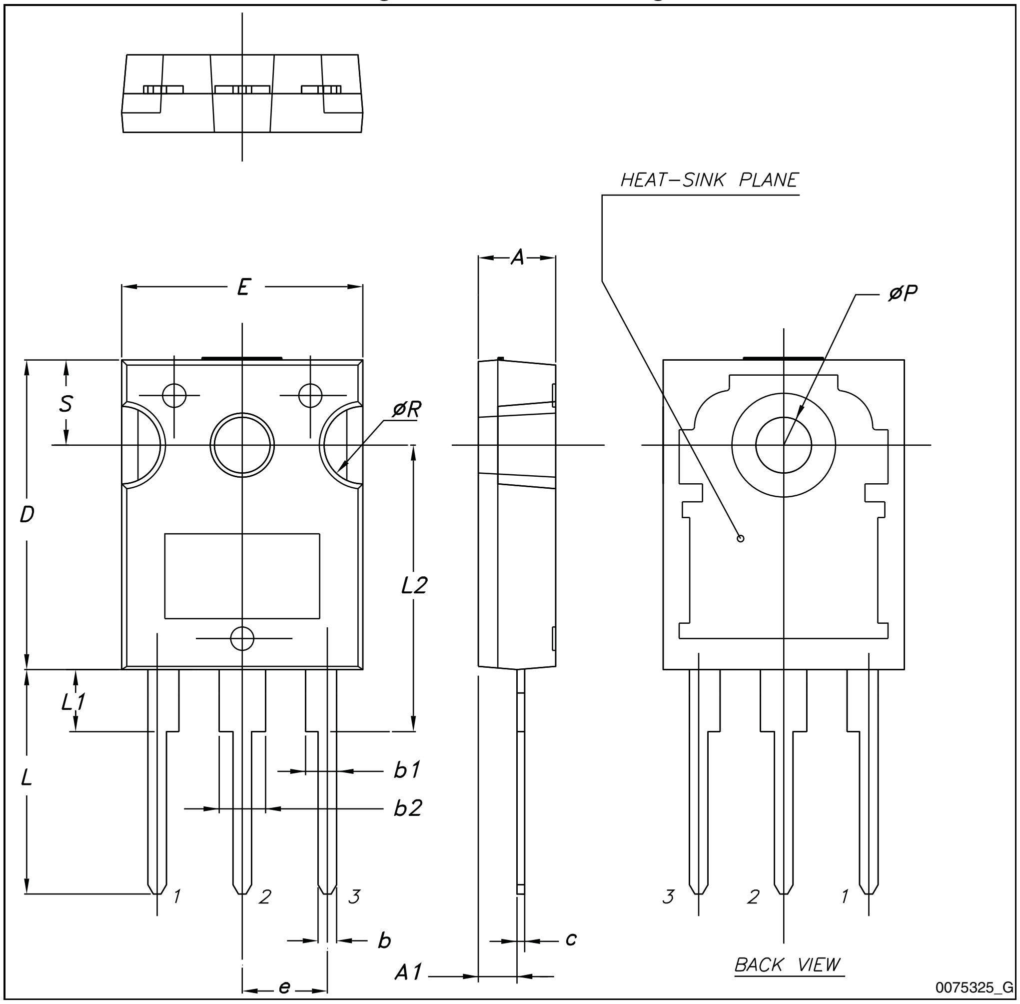


a. All dimensions are in millimeters

Table 9. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
∅P	3.55		3.65
∅R	4.50		5.50
S	5.30	5.50	5.70

Figure 24. TO-247 drawing



5 Packaging mechanical data

Table 10. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 25. Tape

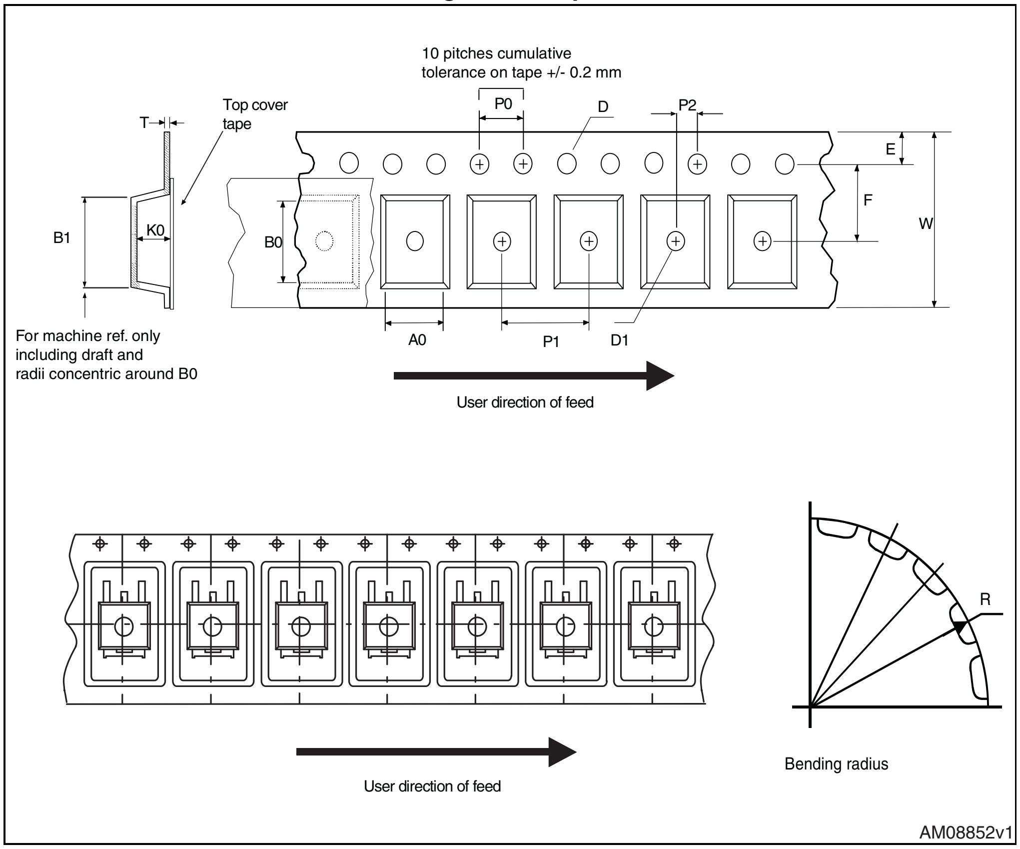
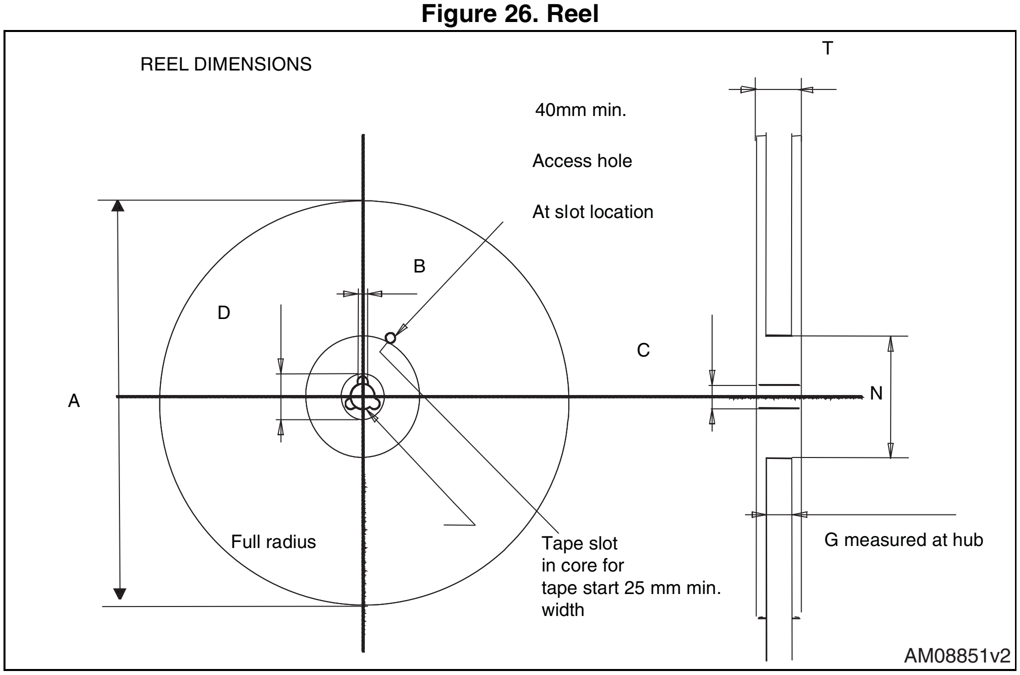


Figure 26. Reel



6 Revision history

Table 11. Document revision history

Date	Revision	Changes
24-Oct-2012	1	Initial release.
01-Jul-2013	2	– Updated *Figure 1: Internal schematic diagram*. – Added *Section 2.1: Electrical characteristics (curves)*.
02-Oct-2013	3	– Modified: E_{AS} in *Table 4*, $C_{oss\ eq.}$ typical value in *Table 6*, *Figure 13* – Minor text changes