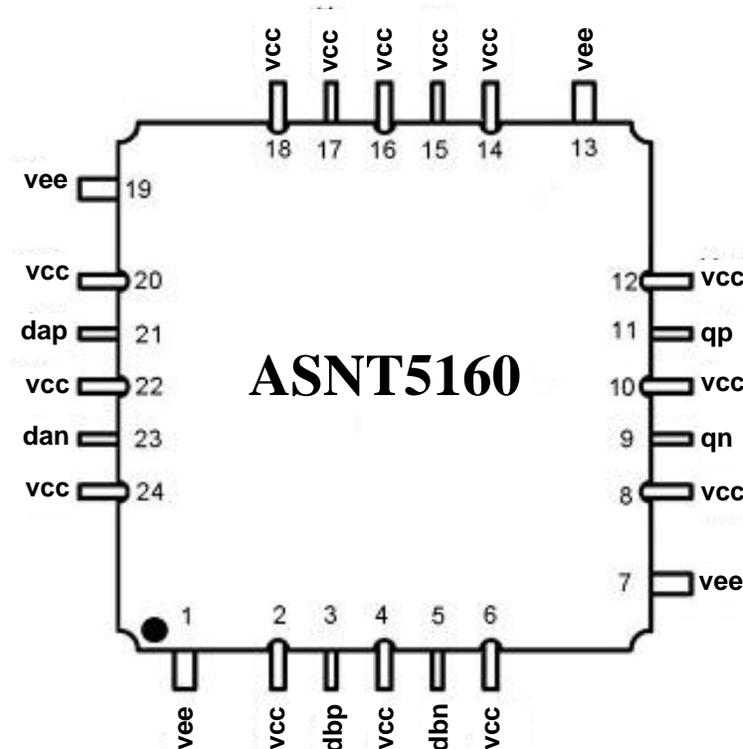




## ASNT5160-KMC DC-50Gbps AND/OR Logic Gate

- High speed broadband AND/OR Boolean logic gate
- Exhibits low jitter and limited temperature variation over industrial temperature range
- 25GHz analog input bandwidth for both data inputs
- Ideal for high speed proof-of-concept prototyping
- Fully differential CML input interfaces
- Fully differential CML output interface with 400mV single-ended swing
- Single +3.3V or -3.3V power supply
- Power consumption: 270mW
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package





## DESCRIPTION

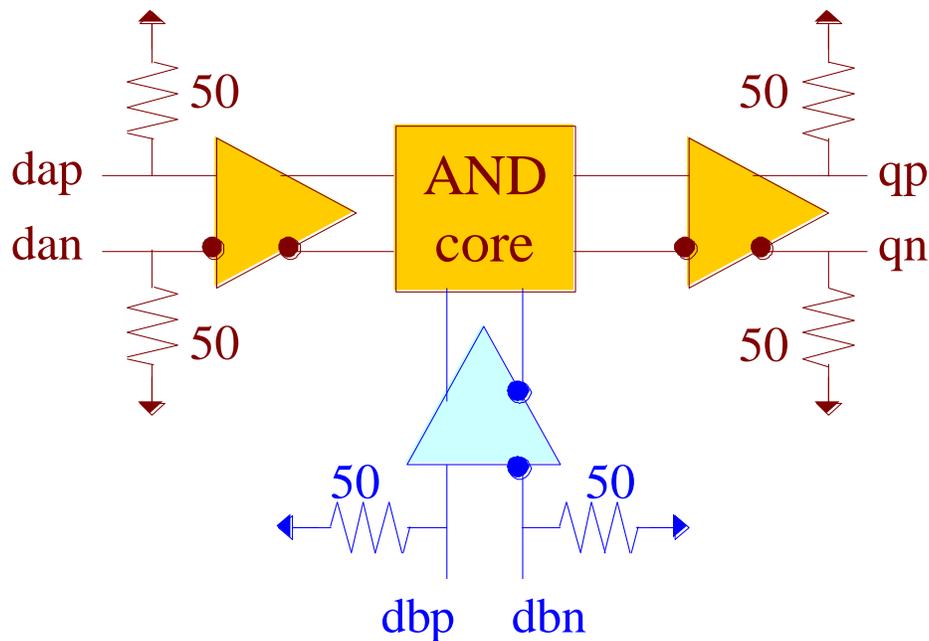


Fig. 1. Functional Block Diagram

The temperature stable ASNT5160-KMC SiGe IC provides broadband AND/OR Boolean logic functionality, and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can AND/OR a high-speed data input signal **dap/dan** with another high-speed data input signal **dbp/dbn**, and deliver a high-speed NRZ data output signal **qp/qn**. An RZ data output signal can be generated by inserting up to half of the IC's maximum data input frequency into one data input signal **dap/dan** or **dbp/dbn** while providing an up to its maximum clock signal analog bandwidth into the other data input **dap/dan** or **dbp/dbn**.

The part's I/O's support the CML logic interface with on chip  $50\Omega$  termination to **vcc** and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

## POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (**vcc** = 0.0V = ground and **vee** = -3.3V), or positive supply (**vcc** = +3.3V and **vee** = 0.0V = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with  $50\Omega$  termination to ground. Different PCB layouts will be needed for each different power supply combination.

**All the characteristics detailed below assume **vcc** = 0.0V and **vee** = -3.3V.**



## ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

| Parameter                   | Min | Max  | Units |
|-----------------------------|-----|------|-------|
| Supply Voltage (vee)        |     | -3.6 | V     |
| Power Consumption           |     | 0.30 | W     |
| RF Input Voltage Swing (SE) |     | 1.0  | V     |
| Case Temperature            |     | +90  | °C    |
| Storage Temperature         | -40 | +100 | °C    |
| Operational Humidity        | 10  | 98   | %     |
| Storage Humidity            | 10  | 98   | %     |

## TERMINAL FUNCTIONS

| TERMINAL                               |                                      |            | DESCRIPTION  |
|--|--------------------------------------|------------|--|
| Name                                   | No.                                  | Type       |  |
| <b>High-Speed I/Os</b>                 |                                      |            |  |
| dap                                    | 21                                   | CML input  | Differential data/clock inputs with internal SE 50Ω termination to VCC.  |
| dan                                    | 23                                   |            |  |
| dbp                                    | 3                                    | CML input  | Differential data/clock inputs with internal SE 50Ω termination to VCC.  |
| dbn                                    | 5                                    |            |  |
| qp                                     | 11                                   | CML output | Differential data outputs with internal SE 50Ω termination to VCC. Require external SE 50Ω termination to VCC. |
| qn                                     | 9                                    |            |  |
| <b>Supply and Termination Voltages</b> |                                      |            |  |
| Name                                   | Description                          |            | Pin Number   |
| vcc                                    | Positive power supply. (+3.3V or 0)  |            | 2, 4, 6, 8, 10, 12, 14, 15, 16, 17, 18, 20, 22, 24   |
| vee                                    | Negative power supply. (0V or -3.3V) |            | 1, 7, 13, 19   |



## ELECTRICAL CHARACTERISTICS

| PARAMETER                                     | MIN     | TYP     | MAX  | UNIT | COMMENTS                           |
|---|---------|---------|------|------|------------------------------------|
| <b>General Parameters</b>                     |         |         |      |      |                                    |
| vee   | -3.1    | -3.3    | -3.5 | V    | ±6%                                |
| vcc   |         | 0.0     |      | V    | External ground                    |
| Ivee  |         | 85      |      | mA   |                                    |
| Power consumption                             |         | 270     |      | mW   |                                    |
| Junction temperature                          | -40     | 25      | 125  | °C   |                                    |
| <b>HS Input Data/Clock (dap/dan, dbp/dbn)</b> |         |         |      |      |                                    |
| Data Rate                                     | DC      |         | 50   | Gbps | When used to generate NRZ data     |
| Clock Frequency                               | DC      |         | 25   | GHz  | When used to generate RZ data      |
| Swing   | 0.05    |         | 1.0  | V    | Differential or SE, p-p            |
| CM Voltage Level                              | vcc-0.8 |         | vcc  | V    | Must match for both inputs         |
| <b>HS Output Data (qp/qn)</b>                 |         |         |      |      |                                    |
| Data Rate                                     | DC      |         | 50   | Gbps |                                    |
| Logic "1" level                               |         | vcc     |      | V    |                                    |
| Logic "0" level                               |         | vcc-0.4 |      | V    | With external 50Ohm DC termination |
| Rise/Fall times                               | 6       | 8       | 10   | ps   | 20%-80%                            |
| Output Jitter                                 |         |         | 1    | ps   | Peak-to-peak                       |

## PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 2. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT5160-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

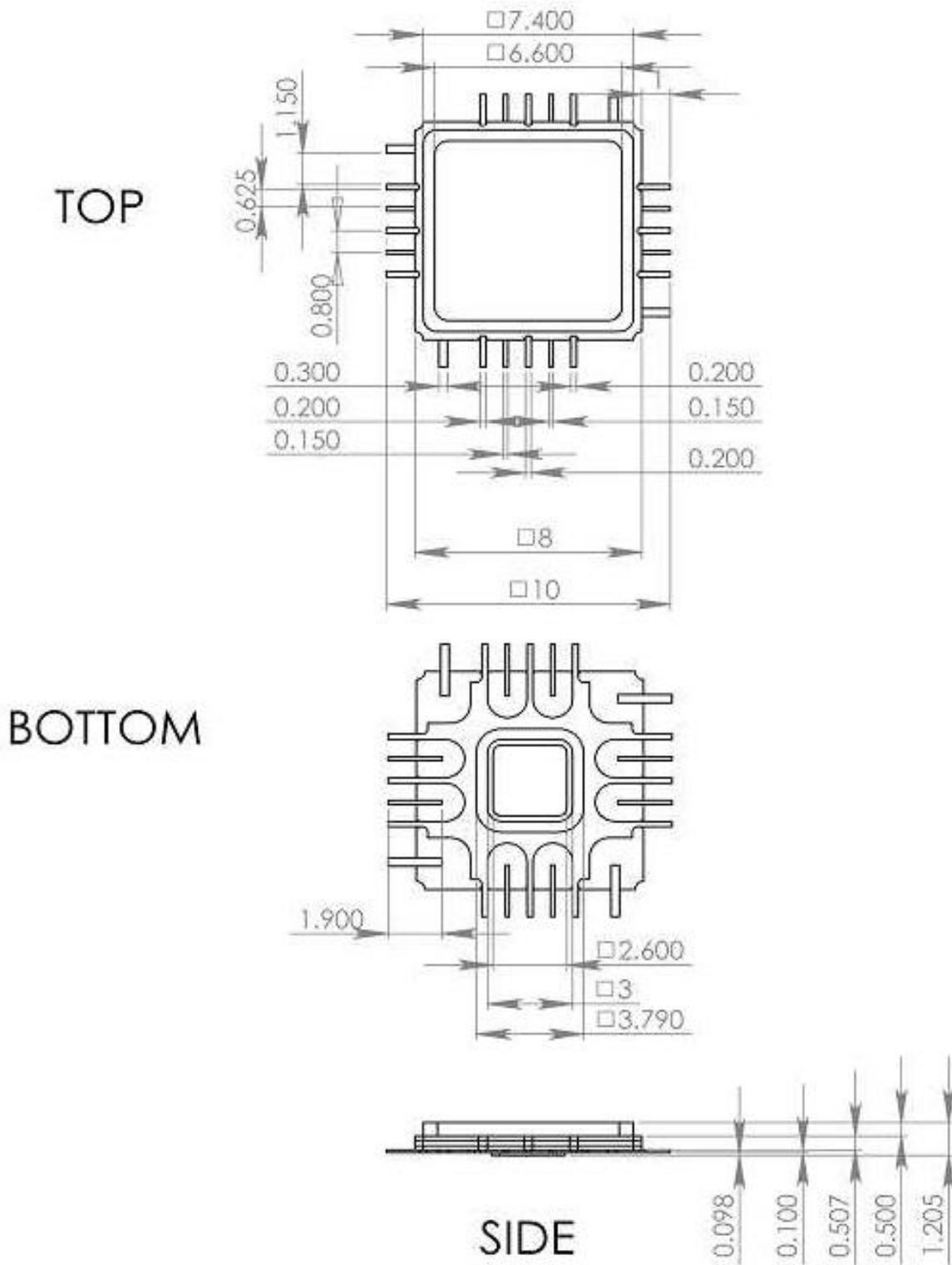


Fig. 2. CQFP 24-Pin Package Drawing (All Dimensions in mm)



## REVISION HISTORY

| Revision | Date    | Changes  |
|----------|---------|--|
| 5.1.2    | 04-2020 | Updated Package Information  |
| 5.0.2    | 07-2019 | Updated Letterhead   |
| 5.0.1    | 03-2013 | Corrected title<br>Added package pin out drawing<br>Revised functional block diagram<br>Revised description<br>Added power supply configuration<br>Added absolute maximum ratings<br>Revised terminal functions<br>Revised electrical characteristics<br>Added package information and mechanical drawing<br>Format correction |
| 4.0      | 02-2008 | Revised electrical characteristics section<br>Revised packaging information section  |
| 3.0      | 06-2007 | Revised electrical characteristics section   |
| 2.0      | 04-2007 | Revised terminal functions section   |
| 1.0      | 01-2007 | First release  |