EVALUATION KIT AVAILABLE

MAX2830

2.4GHz to 2.5GHz 802.11g/b RF Transceiver, PA, and Rx/Tx/Antenna Diversity Switch

General Description

The MAX2830 direct conversion, zero-IF, RF transceiver is designed specifically for 2.4GHz to 2.5GHz 802.11g/b WLAN applications. The MAX2830 completely integrates all circuitry required to implement the RF transceiver function, providing an RF power amplifier (PA), an Rx/Tx and antenna diversity switch, RF-to-baseband receive path, baseband-to-RF transmit path, voltage-controlled oscillator (VCO), frequency synthesizer, crystal oscillator, and baseband/control interface. The MAX2830 includes a fast-settling sigma-delta RF synthesizer with smaller than 20Hz frequency steps and a digitally tuned crystal oscillator allowing use of a low-cost crystal. No I/Q calibration is required; however, the device also integrates on-chip DC-offset cancellation and I/Q errors and carrier leakage-detection circuits for improved performance. Only an RF bandpass filter (BPF), crystal, a pair of baluns, and a small number of passive components are needed to form a complete 802.11g/b WLAN RF front-end solution.

The MAX2830 completely eliminates the need for an external SAW filter by implementing on-chip monolithic filters for both the receiver and transmitter. The baseband filters are optimized to meet the IEEE 802.11g standard and proprietary turbo modes up to 40MHz channel bandwidth. These devices are suitable for the full range of 802.11g OFDM data rates (6Mbps to 54Mbps) and 802.11b QPSK and CCK data rates (1Mbps to 11Mbps). The ICs are available in a small, 48-pin TQFN package measuring only 7mm x 7mm x 0.8mm.

Applications

Wi-Fi, PDA, VOIP, and Cellular Handsets

Wireless Speakers and Headphones

General 2.4GHz ISM Radios

Features

- **2.4GHz to 2.5GHz ISM Band Operation**
- **IEEE 802.11g/b Compatible (54Mbps OFDM and 11Mbps CCK)**
- **Complete RF Transceiver, PA, Rx/Tx and Antenna Diversity Switch, and Crystal Oscillator**
  - **Best-in-Class Transceiver Performance**
  - **62mA Receiver Current**
  - **3.3dB Rx Noise Figure**
  - **-75dBm Rx Sensitivity (54Mbps OFDM)**
  - **No I/Q Calibration Required**
  - **0.1dB/0.35° Rx I/Q Gain/Phase Imbalance**
  - **33dB RF and 62dB Baseband Gain Control Range**
  - **60dB Range Analog RSSI per RF Gain Setting**
  - **Fast Rx I/Q DC-Offset Settling**
  - **Programmable Baseband Lowpass Filter**
  - **20-Bit Sigma-Delta Fractional-N PLL with < 20Hz Step Size**
  - **Digitally Tuned Crystal Oscillator**
  - **+17.1dBm Transmit Power (5.6% EVM with 54Mbps OFDM)**
  - **31dB Tx Gain Control Range**
  - **Integrated Power Detector**
  - **Fully Integrated RF Input and Output Matching and DC Blocking**
  - **Serial or Parallel Gain-Control Interface**
  - **> 40dB Tx Sideband Suppression Without Calibration**
  - **Rx/Tx I/Q Error Detection**
- **Transceiver Operates from +2.7V to +3.6V**
- **PA Operates from +2.7V to +4.2V**
- **Low-Power Shutdown Mode**
- **Small 48-Pin TQFN Package (7mm x 7mm x 0.8mm)**

Selector Guide

PART	INTEGRATED PA	INTEGRATED SWITCH
MAX2830	Yes	Yes
MAX2831	Yes	No
MAX2832	No	No

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2830ETM+T	-40°C to +85°C	48 TQFN-EP*

**EP = Exposed paddle.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Pin Configuration appears at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

V_{CCTXPA}, V_{CCPA}, and ANT__ to GND ....-0.3V to +4.5V
V_{CCLNA}, V_{CCTXMX}, V_{CCPLL}, V_{CCCP}, V_{CCXTAL}, V_{CCVCO}, $V_{CCRXVGA}$, V_{CCRXFL}, and $V_{CCRXMX\_}$ to GND...-0.3V to +3.9V
B6, B7, B3, B2, $\overline{SHDN}$, B5, $\overline{CS}$, SCLK, DIN, B1, TUNE, B4, ANTSEL, TXBBI_, TXBBQ_, RXHP, RXTX, RXBBI_, RXBBQ_, RSSI, BYPASS, CPOUT, LD, CLOCKOUT, XTAL, CTUNE to GND ....-0.3V to (Operating V_{CC} + 0.3V)
RXBBI_, RXBBQ_, RSSI, BYPASS, CPOUT, LD, CLOCKOUT Short-Circuit Duration 10s
RF Input Power...+10dBm
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFN (derates 27.8mW/°C above +70°C) 2.22W
Operating Temperature Range ....-40°C to +85°C
Junction Temperature..+150°C
Storage Temperature Range ....-65°C to +160°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(MAX2830 EV kit, $V_{CC\_}$ = 2.7V to 3.6V, V_{CCPA} = V_{CCTXPA} = 2.7V to 4.2V, T_A = -40°C to +85°C, Rx set to the maximum gain. $\overline{CS}$ = high, RXHP = SCLK = DIN = ANTSEL = low, RSSI and clock output buffer are off, no signal at RF inputs, all RF inputs and outputs terminated into 50Ω, receiver baseband outputs are open. 100mV$_{RMS}$ differential I and Q signals (54Mbps IEEE 802.11g OFDM) applied to I/Q baseband inputs of transmitter in transmit mode, f_{REF} = 40MHz, and registers set to recommended settings and corresponding test mode, unless otherwise noted. Typical values are at V_{CC} = 2.8V, V_{CCPA} = 3.3V, and T_A = +25°C, LO frequency = 2.437GHz, unless otherwise noted. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETERS	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	$V_{CC\_}$		2.7		3.6	V
	V_{CCPA}, V_{CCTXPA}		2.7		4.2	
Supply Current	Shutdown mode, B7: B1 = 0000000, reference oscillator not applied	T_A = +25°C		20		µA
	Standby mode	T_A = +25°C		28	35	mA
		T_A = -40°C to +85°C			35	
	Rx mode	T_A = +25°C		62	78	
		T_A = -40°C to +85°C			82	
	Tx mode, T_A = +25°C, V_{CC} = 2.8V, V_{CCPA} = 3.3V (Note 2)	Transmit section		82	104	
		PA, P_{OUT} = +17.1dBm		212		
	Rx calibration mode	T_A = +25°C		101		
	Tx calibration mode	T_A = +25°C		78		
Rx I/Q Output Common-Mode Voltage	T_A = +25°C at default common-mode setting		0.94	1.2	1.37	V
Rx I/Q Output Common-Mode Voltage Variation	T_A = -40°C (relative to T_A = +25°C)			-17		mV
	T_A = +85°C (relative to T_A = +25°C)			15		
Tx Baseband Input Common-Mode Voltage Operating Range	DC-coupled		0.9		1.3	V
Tx Baseband Input Bias Current	Source current				22	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(MAX2830 EV kit, $V_{CC\_}$ = 2.7V to 3.6V, V_{CCPA} = V_{CCTXPA} = 2.7V to 4.2V, T_A = -40°C to +85°C, Rx set to the maximum gain. $\overline{CS}$ = high, RXHP = SCLK = DIN = ANTSEL = low, RSSI and clock output buffer are off, no signal at RF inputs, all RF inputs and outputs terminated into 50Ω, receiver baseband outputs are open. 100mV$_{RMS}$ differential I and Q signals (54Mbps IEEE 802.11g OFDM) applied to I/Q baseband inputs of transmitter in transmit mode, f_{REF} = 40MHz, and registers set to recommended settings and corresponding test mode, unless otherwise noted. Typical values are at V_{CC} = 2.8V, V_{CCPA} = 3.3V, and T_A = +25°C, LO frequency = 2.437GHz, unless otherwise noted. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS: $\overline{SHDN}$, RXTX, SCLK, DIN, $\overline{CS}$, B7:B1, RXHP, ANTSEL					
Digital Input-Voltage High, V_{IH}		V_{CC} - 0.4			V
Digital Input-Voltage Low, V_{IL}				0.4	V
Digital Input-Current High, I_{IH}		-1		+1	µA
Digital Input-Current Low, I_{IL}		-1		+1	µA
LOGIC OUTPUTS: LD, CLOCKOUT					
Digital Output-Voltage High, V_{OH}	Sourcing 100µA	V_{CC} - 0.4			V
Digital Output-Voltage Low, V_{OL}	Sinking 100µA			0.4	V

AC ELECTRICAL CHARACTERISTICS—Rx Mode

(MAX2830 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A =+25°C, f_{RF} = 2.439GHz, f_{LO} = 2.437GHz; receiver baseband I/Q outputs at 112 mV$_{RMS}$ (-19dBV), f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXTX = SCLK = DIN = low, with power matching for the differential RF pins using the typical applications and registers set to default settings and corresponding test mode, unless otherwise noted. Unmodulated single-tone RF input signal is used with specifications that normally apply over the entire operating conditions, unless otherwise indicated. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RECEIVER SECTION: LNA RF INPUT-TO-BASEBAND I/Q OUTPUTS						
RF Input Frequency Range			2.4		2.5	GHz
RF Input Return Loss (ANT1)	High RF gain			13		dB
	Mid RF gain			16		
	Low RF gain			13		
RF Input Return Loss (ANT2)	High RF gain			21		dB
	Mid RF gain			14		
	Low RF gain			12		
Total Voltage Gain (ANT1)	Maximum gain, B7:B1 = 1111111	T_A = +25°C	86	97		dB
		T_A = -40°C to +85°C	83			
	Minimum gain, B7:B1 = 0000000	T_A = +25°C		2	8	
Total Voltage Gain (ANT2)	Maximum gain, B7:B1 = 1111111	T_A = +25°C		96		dB
	Minimum gain, B7:B1 = 0000000	T_A = +25°C		2		

AC ELECTRICAL CHARACTERISTICS—Rx Mode (continued)

(MAX2830 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A =+25°C, f_{RF} = 2.439GHz, f_{LO} = 2.437GHz; receiver baseband I/Q outputs at 112 mV_{RMS} (-19dBV), f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXTX = SCLK = DIN = low, with power matching for the differential RF pins using the typical applications and registers set to default settings and corresponding test mode, unless otherwise noted. Unmodulated single-tone RF input signal is used with specifications that normally apply over the entire operating conditions, unless otherwise indicated. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF Gain Steps (Note 3)	From high-gain mode (B7:B6 = 11) to medium-gain mode (B7:B6 = 10)			-17		dB
	From high-gain mode (B7:B6 = 11) to low-gain mode (B7:B6 = 0X)			-33.5		
RF Gain-Change Settling Time	Gain change from high gain to medium gain, high gain to low, or medium gain to low gain; gain settling to within ±2dB of steady state; RXHP = 1			0.2		µs
Baseband Gain Range	From maximum baseband gain (B5:B1 = 11111) to minimum baseband gain (B5:B1 = 00000)		54	62	68	dB
DSB Noise Figure (ANT1)	Voltage gain = maximum with B7:B6 = 11			3.3		dB
	Voltage gain = 50dB with B7:B6 = 11			3.8		
	Voltage gain = 45dB with B7:B6 = 10			16.7		
	Voltage gain = 15dB with B7:B6 = 0X			34.7		
DSB Noise Figure (ANT2)	Voltage gain = maximum with B7:B6 = 11			4.0		dB
	Voltage gain = 50dB with B7:B6 = 11			4.5		
	Voltage gain = 45dB with B7:B6 = 10			17.4		
	Voltage gain = 15dB with B7:B6 = 0X			35.3		
In-Band Compression Point Based on EVM	-19dBV_{RMS} baseband output EVM degrades to 9%	B7:B6 = 11		-41		dBm
		B7:B6 = 10		-24		
		B7:B6 = 0X		-6		
In-Band Output P-1dB	Voltage gain = 90dB, with B7:B6 = 11			2.5		V_{P-P}
Out-of-Band Input IP3 (Note 4)	B7:B6 = 11			-12		dBm
	B7:B6 = 10			-4		
	B7:B6 = 0X			24		
I/Q Phase Error	1 σ variation (without calibration)			±0.35		Degrees
I/Q Gain Imbalance	1 σ variation (without calibration)			±0.1		dB
RX I/Q Output Load Impedance (R II C)	Minimum differential resistance			10		kΩ
	Maximum differential capacitance			10		pF
Tx-to-Rx Conversion Gain for Rx I/Q Calibration	For receiver gain, B7:B1 = 1101111 (Note 5)			0.5		dB
Baseband VGA Settling Time	Gain change from B5:B1 = 10111 to B5:B1 = 00111; gain settling to within ±2dB of steady state			0.1		µs
I/Q Output DC Step when RXHP Transitions from 1 to 0 in Presence of 802.11g Short Sequence	After switching RXHP to logic 0 from initial logic 1, during ideal short sequence data at -55dBm input in AWGN channel, for -19dBV output; normalized to RMS signal on I and Q outputs; transition point varied from 0 to 0.8µs in steps of 0.1µs			-5		dBc

AC ELECTRICAL CHARACTERISTICS—Rx Mode (continued)

(MAX2830 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A =+25°C, f_{RF} = 2.439GHz, f_{LO} = 2.437GHz; receiver baseband I/Q outputs at 112 mV_{RMS} (-19dBV), f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXTX = SCLK = DIN = low, with power matching for the differential RF pins using the typical applications and registers set to default settings and corresponding test mode, unless otherwise noted. Unmodulated single-tone RF input signal is used with specifications that normally apply over the entire operating conditions, unless otherwise indicated. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I/Q Output DC Droop	After switching RXHP to 0, D13:D12, Register 7 (A3:A0 = 0111)			±1		V/s
I/Q Static DC Offset	RXHP = 1, B7:B1 = 1101110, 1 σ variation			±1		mV
Spurious Signal Emissions from LNA input	RF = 1GHz to 26.5GHz			-51		dBm
ANT to Receiver Isolation	ANT1 to receiver (in ANT2 mode)			20		dB
	ANT2 to receiver (in ANT1 mode)			47		
RECEIVER BASEBAND FILTERS						
Gain Ripple in Passband	10kHz to 8.5MHz at baseband			±1.3		dB_{P-P}
Group-Delay Ripple in Passband	10kHz to 8.5MHz at baseband			±45		ns_{P-P}
Baseband Filter Rejection (Nominal Mode)	At 8.5MHz			3.2		dB
	At 15MHz			27		
	At 20MHz			50		
	At > 40MHz			80		
RSSI						
RSSI Minimum Output Voltage	R_{LOAD} ≥ 10kΩ ll 5pF			0.4		V
RSSI Maximum Output Voltage	R_{LOAD} ≥ 10kΩ ll 5pF			2.4		V
RSSI Slope				30		mV/dB
RSSI Output Settling Time	To within 3dB of steady state	+32dB signal step		200		ns
		-32dB signal step		600		

AC ELECTRICAL CHARACTERISTICS—Tx Mode

(MAX2830 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{RF} = 2.439GHz , f_{LO} = 2.437GHz. f_{REF} = 40MHz, $\overline{SHDN}$ = RXTX = $\overline{CS}$ = ANTSEL = high, and SCLK = DIN = low, with power matching for the differential RF pins using the typical applications circuit. 100mV$_{RMS}$ sine and cosine signal (or 100mV$_{RMS}$ 54Mbps IEEE 802.11g I/Q signals wherever OFDM is mentioned) applied to baseband I/Q inputs of transmitter (differential DC-coupled). Registers set to recommend settings and corresponding test mode, unless otherwise noted. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TRANSMIT SECTION: Tx BASEBAND I/Q INPUTS TO RF OUTPUTS						
RF Output Frequency Range			2.4		2.5	GHz
Output Power	54Mbps 802.11g OFDM signal	Output power adjusted to meet 5.6%EVM, and spectral mask		17.1		dBm
	6Mbits, OFDM, I/Q signals	Output power adjusted to meet spectral mask		20.3		
Gain Control Range	B6:B1 = 000000 to 111000			26		dB
Unwanted Sideband Suppression	Without I/Q calibration, B6:B1 = 100001			-42		dBc
Carrier Leakage at Center Frequency of Channel	Without DC offset correction			-30		dBc
Transmitter Spurious Signal Emissions	B6:B1 = 111000, OFDM signal	1/3 x f_{LO}		-67		dBm/MHz
		< 1GHz		-36		
		> 1GHz		-47		
		2/3 x f_{LO}		-64		
		4/3 x f_{LO}		-42		
		5/3 x f_{LO}		-65		
		8/3 x f_{LO}		-55		
		2 x f_{LO}		-27		
		3 x f_{LO}		-54		
RF Output Return Loss	Off-chip balun and single ended			-15		dB
Tx I/Q Input Load Impedance (R ll C)	Minimum differential resistance			20		kΩ
	Maximum differential capacitance			0.7		pF
Baseband -3dB Corner Frequency	D1:D0 = 01, Register 8 (A3:A0 = 1000)	Nominal mode		11		MHz
Baseband Filter Rejection	At 30MHz, in nominal mode			62		dB
Minimum Power-Detector Output Voltage	Short sequence transmitter power = +10dBm			0.35		V
Maximum Power-Detector Output Voltage	Short sequence transmitter power = +20dBm			1.2		V
RF Power-Detector Response Time				0.3		µs

AC ELECTRICAL CHARACTERISTICS—Tx Mode (continued)

(MAX2830 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{RF} = 2.439GHz , f_{LO} = 2.437GHz. f_{REF} = 40MHz, $\overline{SHDN}$ = RXTX = $\overline{CS}$ = ANTSEL = high, and SCLK = DIN = low, with power matching for the differential RF pins using the typical applications circuit. 100mV_{RMS} sine and cosine signal (or 100mV_{RMS} 54Mbps IEEE 802.11g I/Q signals wherever OFDM is mentioned) applied to baseband I/Q inputs of transmitter (differential DC-coupled). Registers set to recommend settings and corresponding test mode, unless otherwise noted. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TRANSMITTER LO LEAKAGE AND I/Q CALIBRATION USING LO LEAKAGE AND SIDEBAND DETECTOR (see the *Rx/Tx Calibration Mode* section)						
Tx BASEBAND I/Q INPUTS TO RECEIVER OUTPUTS						
LO Leakage and Sideband Detector Output	Calibration register, D12:D11 = 00, A3:A0 = 0110	Output at 1 x f_{TONE} (for LO leakage = -29dBc), f_{TONE} = 2MHz, 100mV_{RMS}		-34		dBV_{RMS}
		Output at 2 x f_{TONE} (for LO leakage = -240dBc), f_{TONE} = 2MHz, 100mV_{RMS}		-44		
Amplifier Gain Range	D12:D11 = 00 to D12:D11 = 11, A3:A0 = 0110			30		dB
Lower -3dB Corner Frequency				1		MHz

AC ELECTRICAL CHARACTERISTICS—Frequency Synthesizer

(MAX2830 EV kit, $V_{CC\_}$ = 2.7V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, SCLK = DIN = low, PLL loop bandwidth = 150kHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FREQUENCY SYNTHESIZER						
RF Channel Center Frequency			2.4		2.5	GHz
Channel Center Frequency Programming Minimum Step Size				20		Hz
Charge-Pump Comparison Frequency				20		MHz
Reference Frequency Range			20		44	MHz
Reference Frequency Input Levels	AC-coupled to XTAL pin		800			mV_{P-P}
Reference Frequency Input Impedance (R II C)	Resistance (XTAL)			5		kΩ
	Capacitance (XTAL)			4		pF
Closed-Loop Phase Noise	f_{OFFSET} = 1kHz			-86		dBc/Hz
	f_{OFFSET} = 10kHz			-94		
	f_{OFFSET} = 100kHz			-94		
	f_{OFFSET} = 1MHz			-110		
	f_{OFFSET} = 10MHz			-120		
Closed-Loop Integrated Phase Noise	RMS phase jitter; integrate from 10kHz to 10MHz offset			0.9		Degrees
Charge-Pump Output Current				1		mA
Reference Spurs	20MHz offset			-55		dBc
VCO Frequency Error	Measured from Tx-Rx or Rx-Tx transition	3µs to 9µs		50		kHz
		> 9µs		1		
VOLTAGE-CONTROLLED OSCILLATOR						
Pushing	Referred to 2400MHz LO, V_{CC} varies by 0.3V			210		kHz
LO Tuning Gain	V_{TUNE} = 0.5V			103		MHz/V
	V_{TUNE} = 2.2V			86		

AC ELECTRICAL CHARACTERISTICS—Miscellaneous Blocks

(MAX2830 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, f_{LO} = 2.437GHZ, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, SCLK = DIN = low, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CRYSTAL OSCILLATOR						
On-Chip Tuning Capacitance Range	Maximum capacitance, A3:A0 = 1110, D6:D0 = 1111111			15.4		pF
	Minimum capacitance, A3:A0 = 1110, D6:D0 = 0000000			0.5		
On-Chip Tuning Capacitance Step Size				0.12		pF
ON-CHIP TEMPERATURE SENSOR						
Output Voltage	A3:A0 = 1000, D9:D8 = 01	T_A = -40°C		0.35		V
		T_A = +25°C		1		
		T_A = +85°C		1.6		

AC ELECTRICAL CHARACTERISTICS—Timing

(MAX2830 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A =+25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, SCLK = DIN = low, PLL loop bandwidth = 150kHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SYSTEM TIMING (see Figure 3)						
Turn-On Time	From $\overline{SHDN}$ rising edge to LO settled within 1kHz using external reference frequency input			60		µs
Crystal Oscillator Turn-On Time	90% of final output amplitude level			1		ms
Channel Switching Time	Loop BW = 150kHz, f_{RF} = 2.5GHz to 2.4GHz			25		µs
Rx/Tx Turnaround Time	Measured from Tx or Rx enable rising edge; signal settling to within ±2dB of steady state	Rx to Tx		2		µs
		Tx to Rx, RXHP = 1		2		
Tx Turn-On Time (from Standby Mode)	From Tx-enable active rising edge; signal settling to within ±2dB of steady state			1.5		µs
Tx Turn-Off Time (from Standby Mode)	From Tx-enable inactive rising edge			1		µs
Rx Turn-On Time (from Standby Mode)	From Rx-enable active rising edge; signal settling to within ±2dB of steady state			1.9		µs
Rx Turn-Off Time (from Standby Mode)	From Rx-enable inactive rising edge			0.1		µs

AC ELECTRICAL CHARACTERISTICS—Timing (continued)

(MAX2830 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A =+25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, SCLK = DIN = low, PLL loop bandwidth = 150kHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

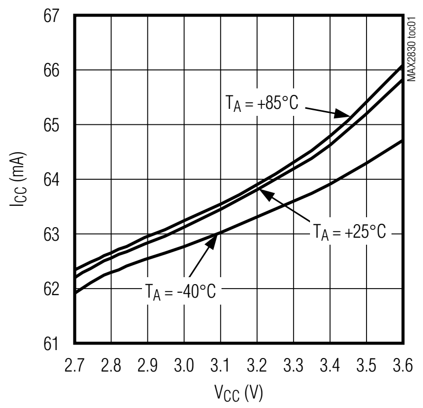
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
3-WIRE SERIAL-INTERFACE TIMING (see Figure 2)					
SCLK Rising Edge to $\overline{CS}$ Falling Edge Wait Time, t_{CSO}			6		ns
Falling Edge of $\overline{CS}$ to Rising Edge of First SCLK Time, t_{CSS}			6		ns
DIN to SCLK Setup Time, t_{DS}			6		ns
DIN to SCLK Hold Time, t_{DH}			6		ns
SCLK Pulse-Width High, t_{CH}			6		ns
SCLK Pulse-Width Low, t_{CL}			6		ns
Last Rising Edge of SCLK to Rising Edge of $\overline{CS}$ or Clock to Load Enable Setup Time, t_{CSH}			6		ns
$\overline{CS}$ High Pulse Width, t_{CSW}			20		ns
Time Between the Rising Edge of $\overline{CS}$ and the Next Rising Edge of SCLK, t_{CS1}			6		ns
Clock Frequency, f_{CLK}			20		MHz
Rise Time, t_R			2		ns
Fall Time, t_F			2		ns

Note 1: Min and max limits are guaranteed by test above T_A = +25°C and guaranteed by design and characterization at T_A = -40°C. The power-on register settings are not production tested. Recommended register setting must be loaded after V_{CC} is supplied.
Note 2: Guaranteed by design and characterization.
Note 3: The nominal part-to-part variation of the RF gain step is ±1dB.
Note 4: Two tones at +25MHz and +48MHz offset with -35dBm/tone. Measure IM3 at 2MHz.
Note 5: Tx I/Q inputs = $100mV_{RMS}$.

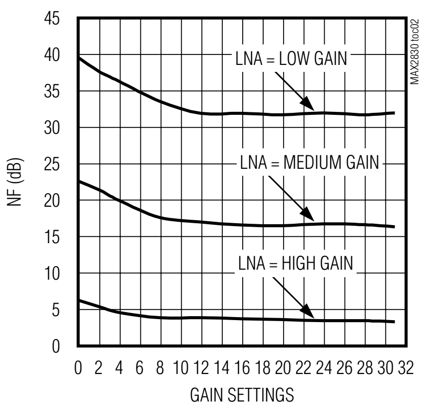
Typical Operating Characteristics

(MAX2830 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low.)

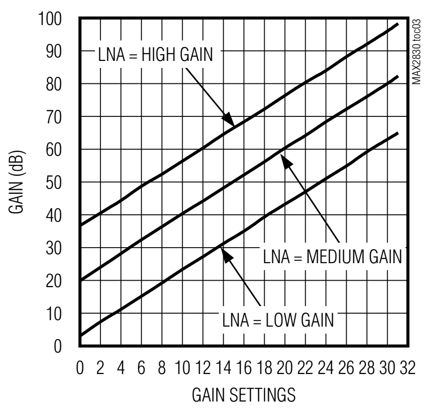
Rx I_{CC} vs. V_{CC}



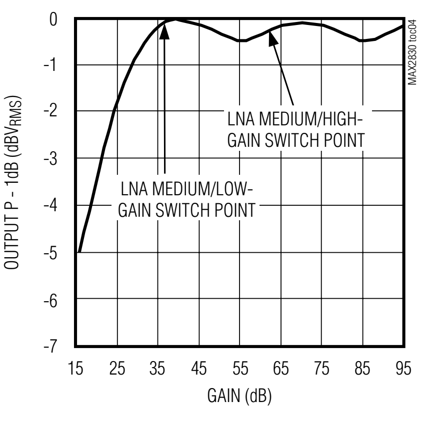
NOISE FIGURE vs. BASEBAND GAIN SETTINGS



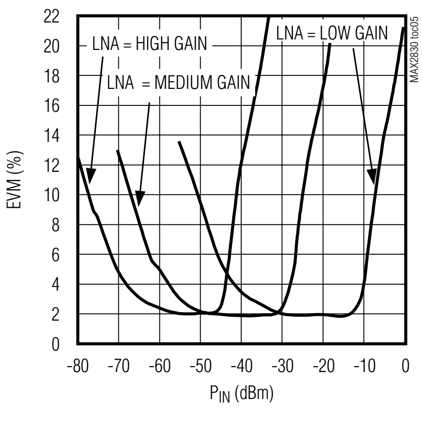
Rx VOLTAGE GAIN vs. BASEBAND GAIN SETTING



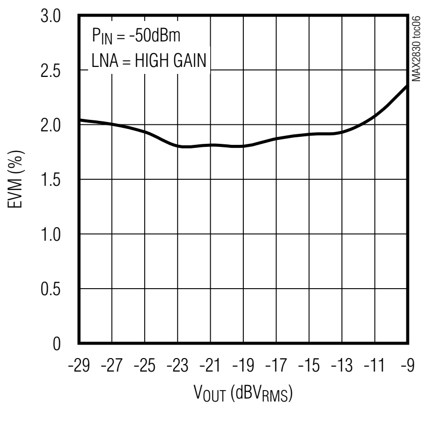
Rx IN-BAND OUTPUT P - 1dB vs. GAIN



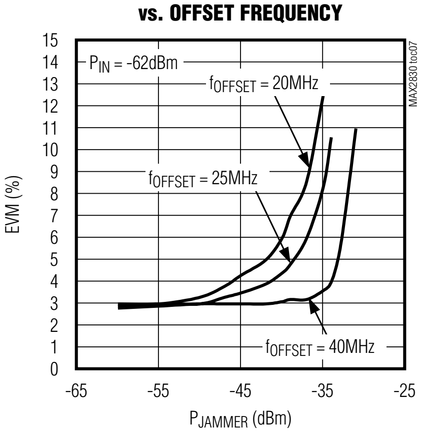
Rx EVM vs. P_{IN}



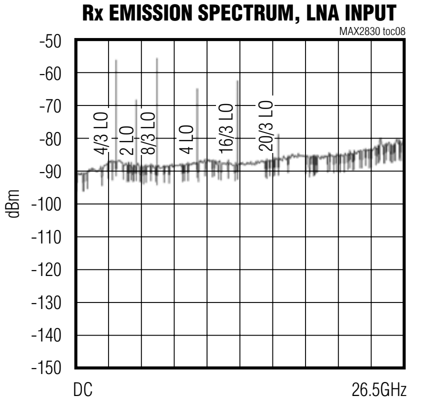
Rx EVM vs. V_{OUT}



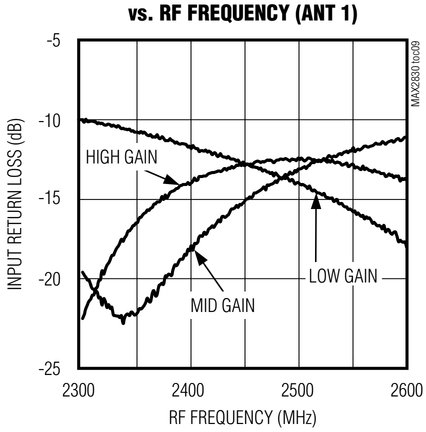
OFDM EVM WITH OFDM JAMMER vs. OFFSET FREQUENCY



Rx EMISSION SPECTRUM, LNA INPUT



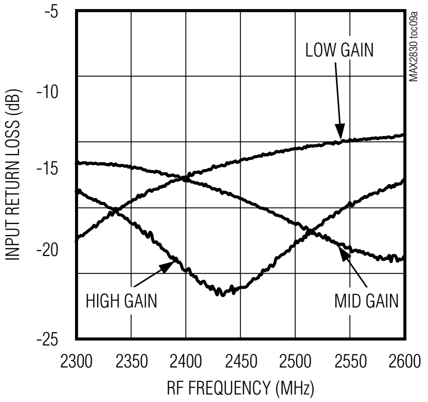
LNA INPUT RETURN LOSS vs. RF FREQUENCY (ANT 1)



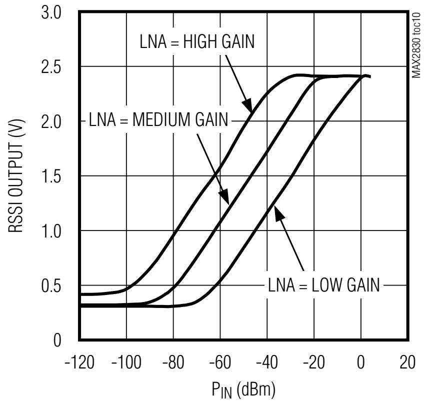
Typical Operating Characteristics (continued)

(MAX2830 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low.)

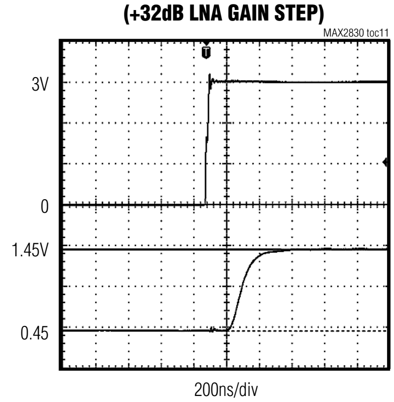
LNA INPUT RETURN LOSS vs. RF FREQUENCY (ANT 2)



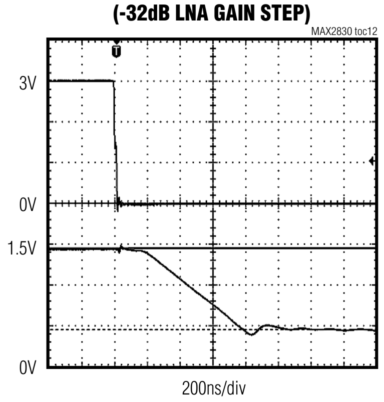
Rx RSSI OUTPUT vs. INPUT POWER



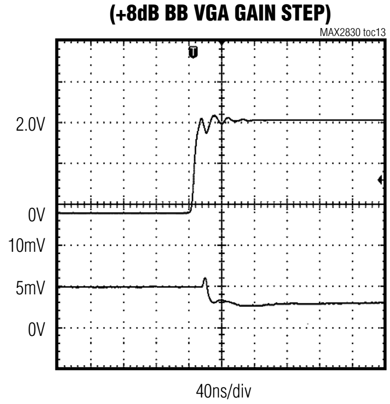
Rx RSSI STEP RESPONSE (+32dB LNA GAIN STEP)



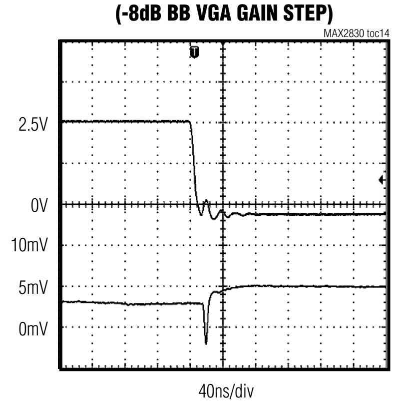
Rx RSSI STEP RESPONSE (-32dB LNA GAIN STEP)



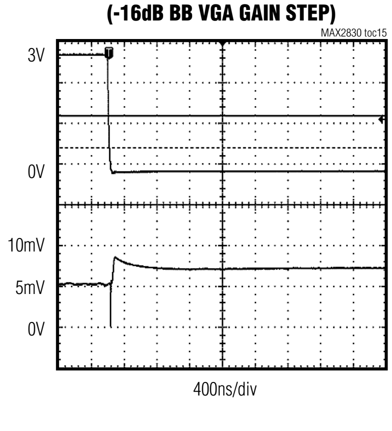
Rx I/Q DC OFFSET SETTLING RESPONSE (+8dB BB VGA GAIN STEP)



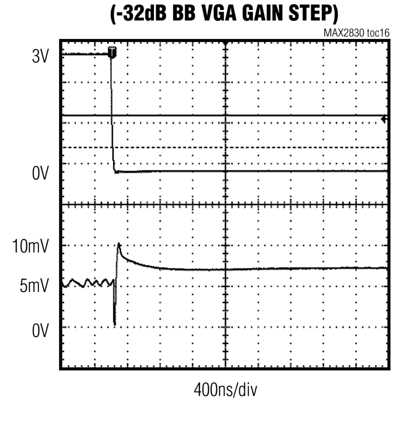
Rx I/Q DC OFFSET SETTLING RESPONSE (-8dB BB VGA GAIN STEP)



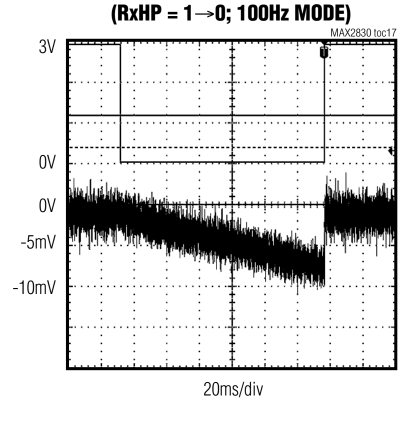
Rx I/Q DC OFFSET SETTLING RESPONSE (-16dB BB VGA GAIN STEP)



Rx I/Q DC OFFSET SETTLING RESPONSE (-32dB BB VGA GAIN STEP)



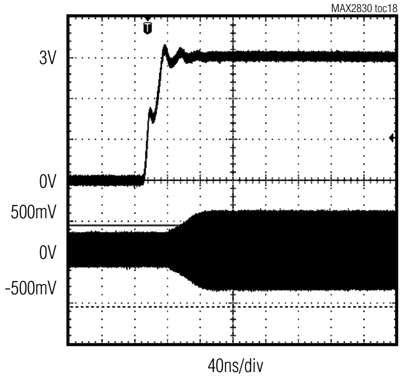
I/Q OUTPUT DC ERROR DROOP (RxHP = 1→0; 100Hz MODE)



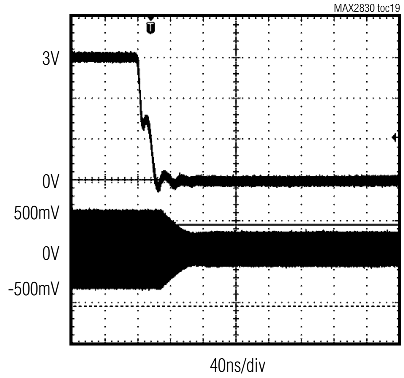
Typical Operating Characteristics (continued)

(MAX2830 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low.)

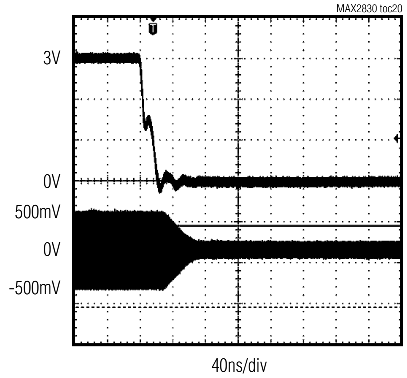
Rx BB VGA SETTLING RESPONSE (+8 GAIN STEP)



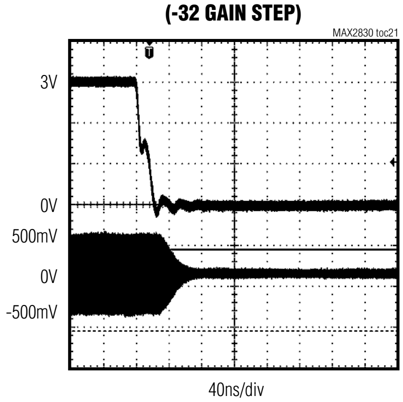
Rx BB VGA SETTLING RESPONSE (-8 GAIN STEP)



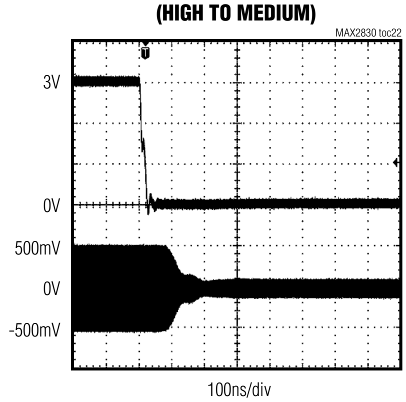
Rx BB VGA SETTLING RESPONSE (-16 GAIN STEP)



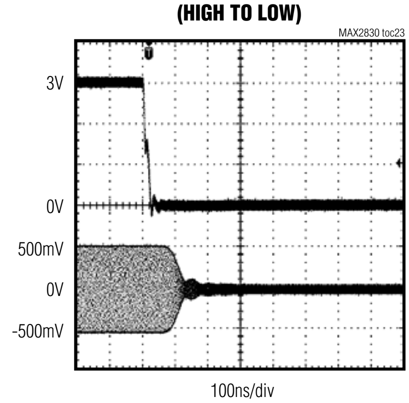
Rx BB VGA SETTLING RESPONSE (-32 GAIN STEP)



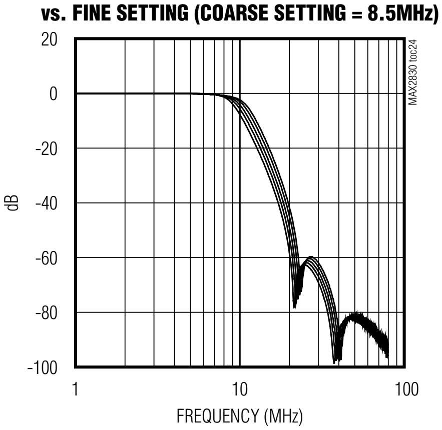
RF LNA SETTLING RESPONSE (HIGH TO MEDIUM)



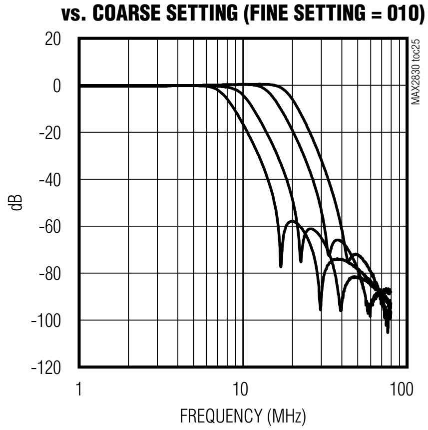
RF LNA SETTLING RESPONSE (HIGH TO LOW)



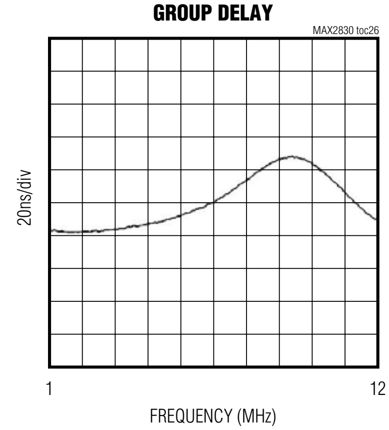
Rx BB FREQUENCY RESPONSE vs. FINE SETTING (COARSE SETTING = 8.5MHz)



Rx BB FREQUENCY RESPONSE vs. COARSE SETTING (FINE SETTING = 010)



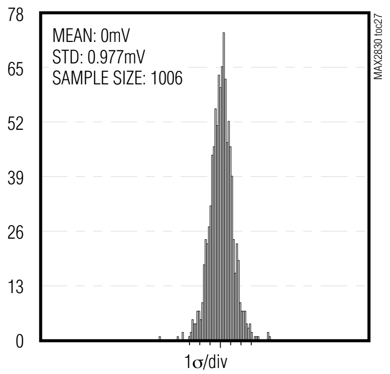
Rx BASEBAND FILTER GROUP DELAY



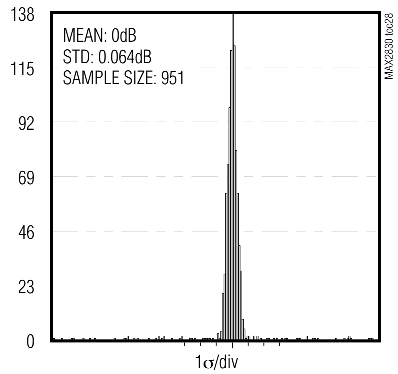
Typical Operating Characteristics (continued)

(MAX2830 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low.)

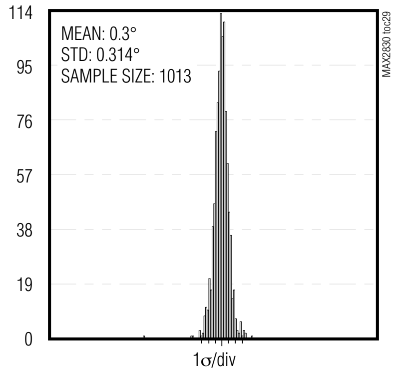
HISTOGRAM: Rx STATIC DC OFFSET



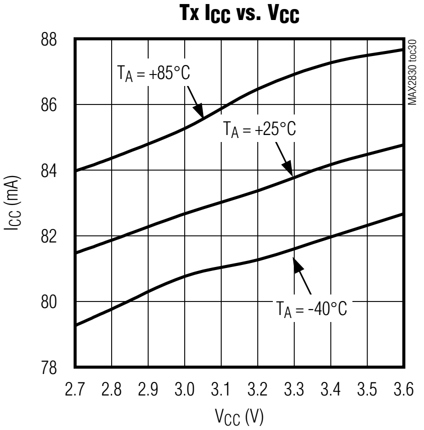
HISTOGRAM: Rx GAIN IMBALANCE



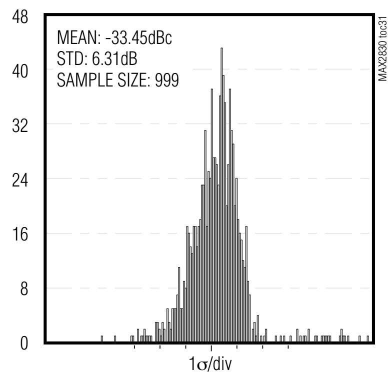
HISTOGRAM: Rx PHASE IMBALANCE



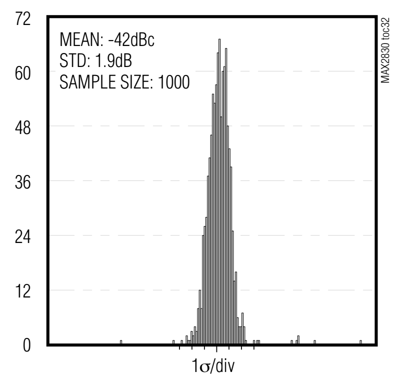
Tx I_{CC} vs. V_{CC}



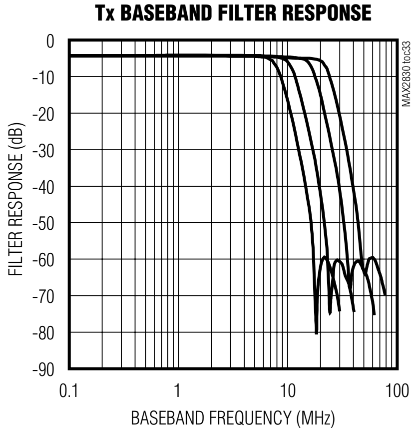
HISTOGRAM: Tx LO LEAKAGE



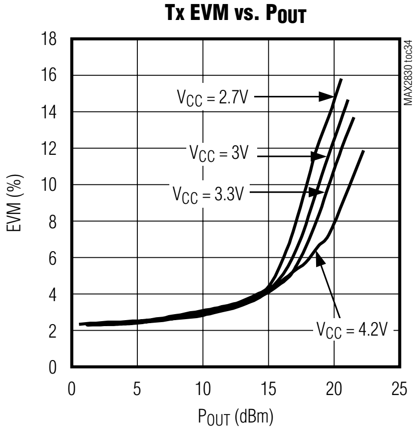
HISTOGRAM: Tx SIDEBAND SUPPRESSION



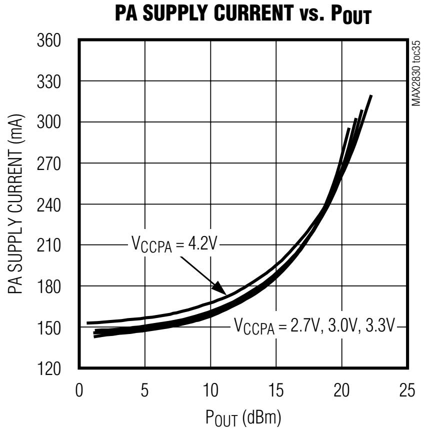
Tx BASEBAND FILTER RESPONSE



Tx EVM vs. P_{OUT}



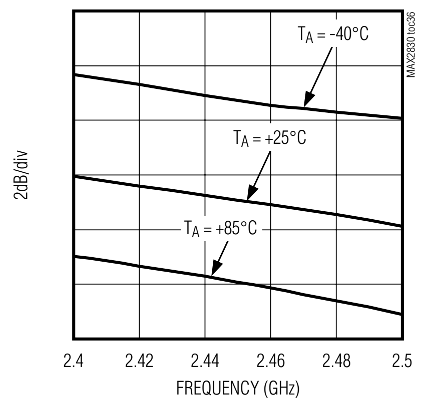
PA SUPPLY CURRENT vs. P_{OUT}



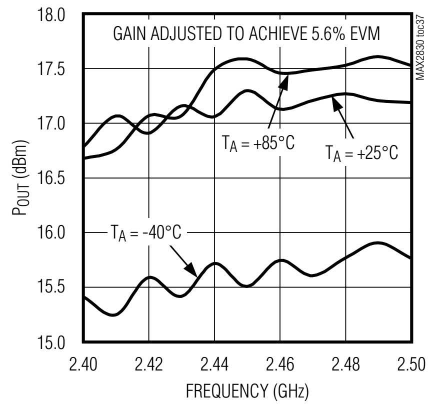
Typical Operating Characteristics (continued)

(MAX2830 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low.)

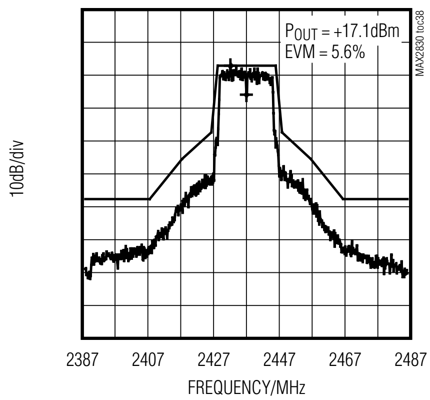
Tx GAIN VARIATION vs. FREQUENCY (B6:B1 = 101001)



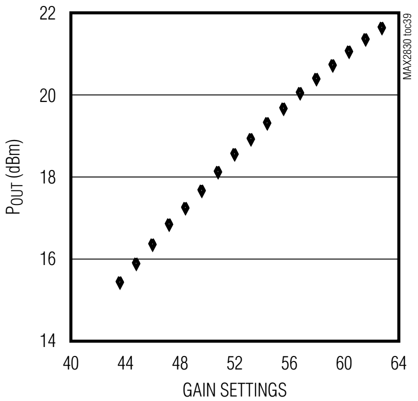
Tx OUTPUT POWER vs. FREQUENCY



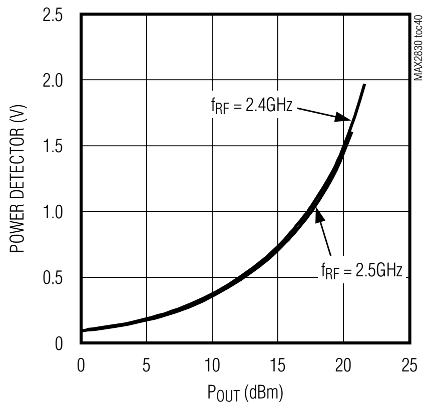
TRANSMIT EMISSION MASK



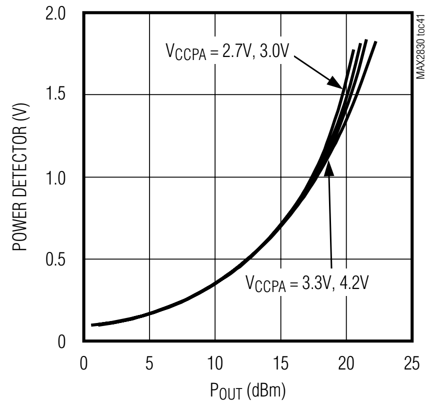
802.11g P_{OUT} vs. GAIN SETTING (UPPER GAIN CONTROL RANGE)



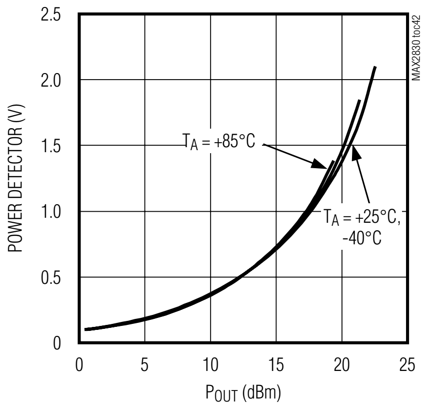
POWER DETECTOR OVER FREQUENCY



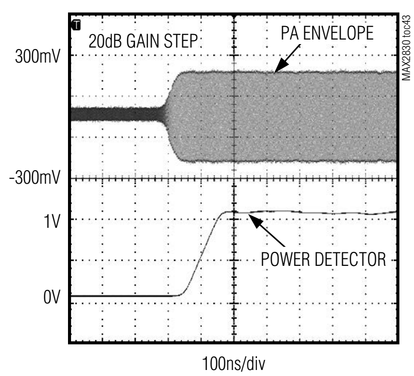
POWER DETECTOR OVER SUPPLY VOLTAGE



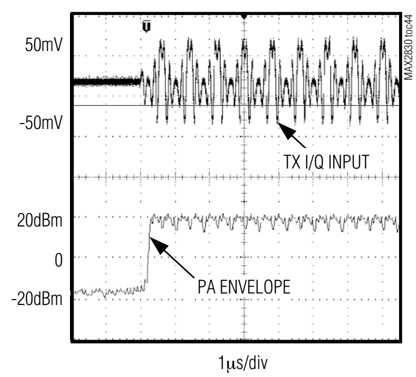
POWER DETECTOR OVER TEMPERATURE



POWER-DETECTOR OUTPUT



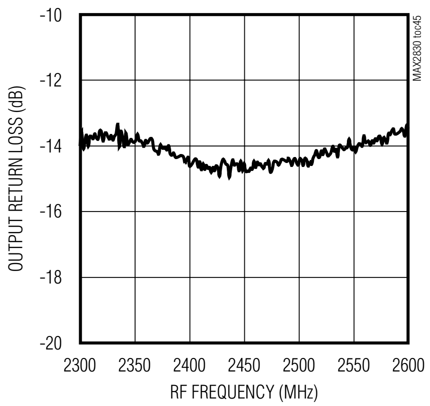
PA OUTPUT ENVELOPE RESPONSE



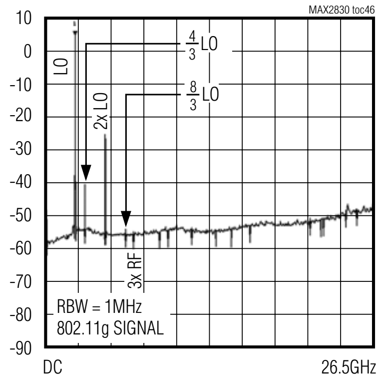
Typical Operating Characteristics (continued)

(MAX2830 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low.)

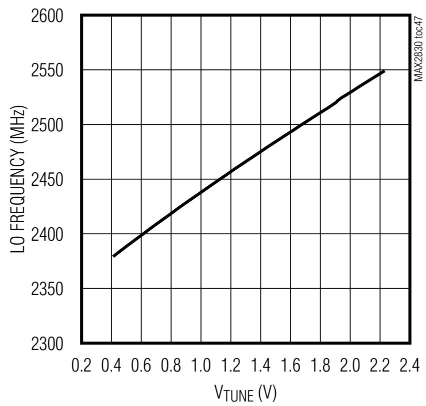
PA OUTPUT RETURN LOSS vs. RF FREQUENCY



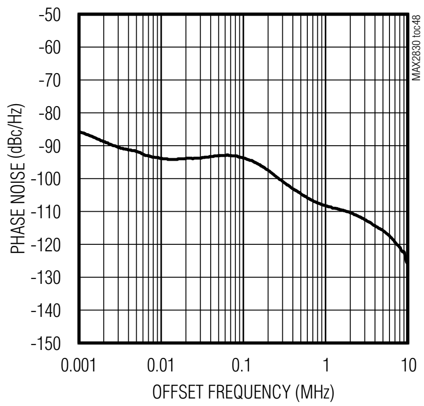
Tx OUTPUT SPURS



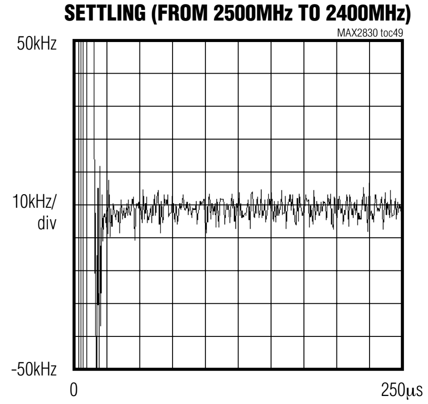
LO FREQUENCY vs. V_{TUNE}



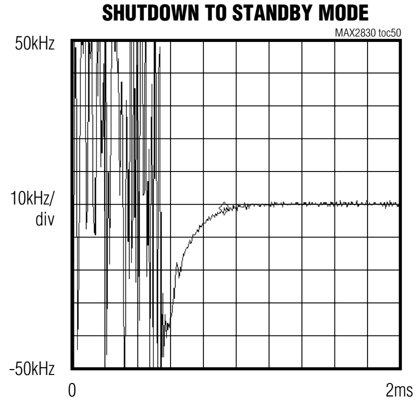
LO PHASE NOISE vs. OFFSET FREQUENCY



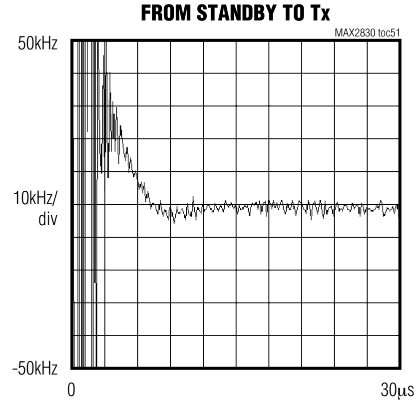
CHANNEL SWITCHING FREQUENCY SETTLING (FROM 2500MHz TO 2400MHz)



PLL SETTLING TIME FROM SHUTDOWN TO STANDBY MODE

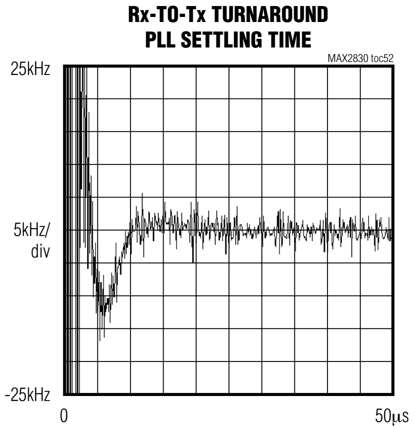


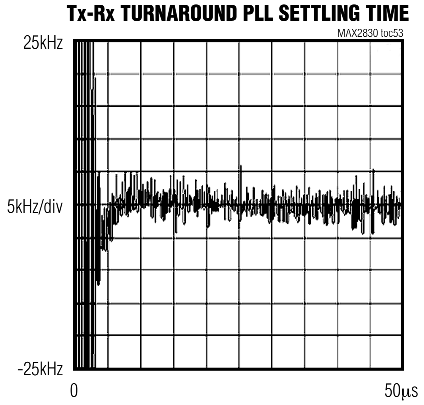
PLL SETTLING TIME FROM STANDBY TO Tx

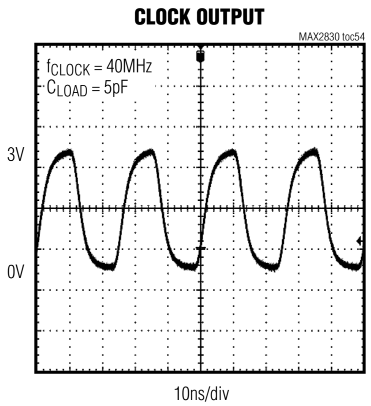


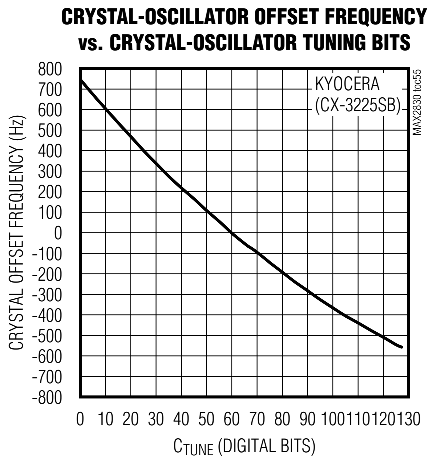
Typical Operating Characteristics (continued)

(MAX2830 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low.)

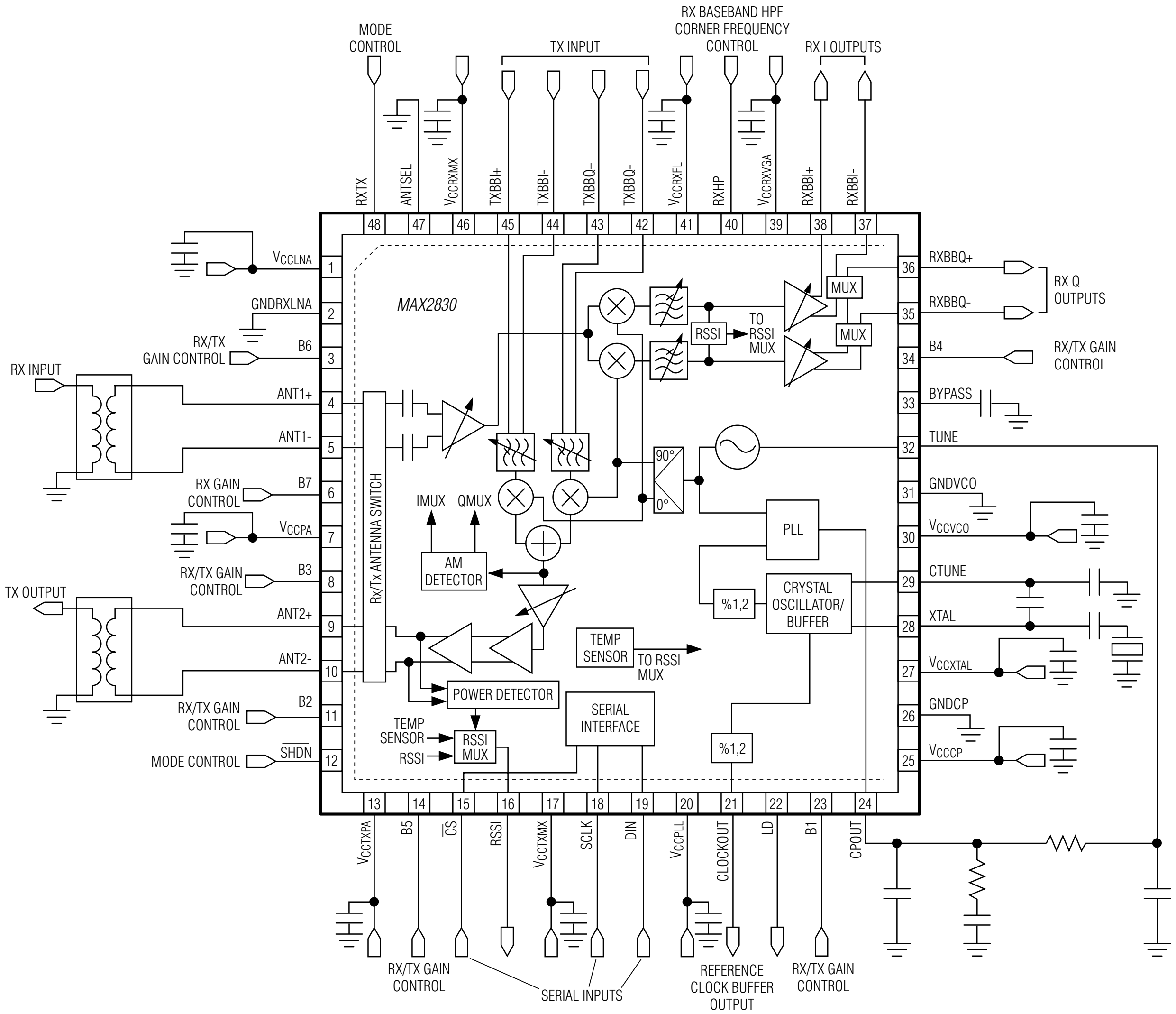








Block Diagram/Typical Operating Circuit



NOTE: ALL GROUND PINS (PINS 2, 26, AND 31) AND BYPASS CAPACITORS' GROUND REQUIRE THEIR OWN VIAS TO GROUND.
DO NOT CONNECT THEM TO THE EXPOSED PADDLE GROUND.

Pin Description

PIN	NAME	FUNCTION
1	V_{CCLNA}	LNA Supply Voltage
2	GNDRXLNA	LNA Ground
3	B6	Receiver and Transmitter Gain-Control Logic-Input Bit 6
4	ANT1+	Antenna 1. Differential Input to LNA in Rx mode. Input is internally AC-coupled and matched to 100Ω differential. Connect directly to a 2:1 balun.
5	ANT1-	
6	B7	Receiver Gain-Control Logic-Input Bit 7
7	V_{CCPA}	Supply Voltage for Second Stage of Power Amplifier
8	B3	Receiver and Transmitter Gain-Control Logic-Input Bit 3
9	ANT2+	Antenna 2. Differential inputs to LNA in diversity Rx mode and to PA differential outputs in Tx mode. Internally AC-coupled differential outputs and matched to 100Ω differential. Connect directly to a 2:1 balun.
10	ANT2-	
11	B2	Receiver and Transmitter Gain-Control Logic-Input Bit 2
12	$\overline{SHDN}$	Active-Low Shutdown and Standby Logic Input. See Table 32 for operating modes.
13	V_{CCTXPA}	Supply Voltage for First-Stage of PA and PA Driver
14	B5	Receiver and Transmitter Gain-Control Logic-Input Bit 5
15	$\overline{CS}$	Active-Low Chip-Select Logic Input of 3-Wire Serial Interface (see Figure 3)
16	RSSI	RSSI, PA Power Detector or Temperature-Sensor Multiplexed Analog Output
17	V_{CCTXMX}	Transmitter Upconverter Supply Voltage
18	SCLK	Serial-Clock Logic Input of 3-Wire Serial Interface (see Figure 3)
19	DIN	Data Logic Input of 3-Wire Serial Interface (see Figure 3)
20	V_{CCPLL}	PLL and Registers Supply Voltage. Connect to the supply voltage to retain the register settings.
21	CLOCKOUT	Reference Clock Buffer Output
22	LD	Lock-Detect Logic Output of Frequency Synthesizer. Output high indicates that the frequency synthesizer is locked. Output programmable as CMOS or open-drain output. (See Tables 17 and 21.)
23	B1	Receiver and Transmitter Gain-Control Logic-Input Bit 1
24	CPOUT	Charge-Pump Output. Connect the frequency synthesizer's loop filter between CPOUT and TUNE (see the *Block Diagram/Typical Operating Circuit*).
25	V_{CCCP}	PLL Charge-Pump Supply Voltage
26	GNDCP	Charge-Pump Circuit Ground
27	V_{CCXTAL}	Crystal Oscillator Supply Voltage
28	XTAL	Crystal or Reference Clock Input. AC-couple a crystal or a reference clock to this analog input.
29	CTUNE	Connection for Crystal Oscillator Off-Chip Capacitors. When using an external reference clock input, leave CTUNE unconnected.
30	V_{CCVCO}	VCO Supply Voltage
31	GNDVCO	VCO Ground
32	TUNE	VCO TUNE Input (see the *Block Diagram/Typical Operating Circuit*)
33	BYPASS	On-Chip VCO Regulator Output Bypass. Bypass with a 0.1µF to 1µF capacitor to GND. Do not connect other circuitry to this point.
34	B4	Receiver and Transmitter Gain-Control Logic-Input Bit 4

Pin Description (continued)

PIN	NAME	FUNCTION
35	RXBBQ-	Receiver Baseband Q-Channel Differential Outputs. In TX calibration mode, these pins are the LO leakage and sideband detector outputs.
36	RXBBQ+	
37	RXBBI-	Receiver Baseband I-Channel Differential Outputs. In TX calibration mode, these pins are the LO leakage and sideband detector outputs.
38	RXBBI+	
39	$V_{CCRXVGA}$	Receiver VGA Supply Voltage
40	RXHP	Receiver Baseband AC-Coupling High-Pass Corner Frequency Control Logic Input
41	V_{CCRXFL}	Receiver Baseband Filter Supply Voltage
42	TXBBQ-	Transmitter Baseband I-Channel Differential Inputs
43	TXBBQ+	
44	TXBBI-	Transmitter Baseband Q-Channel Differential Inputs
45	TXBBI+	
46	V_{CCRXMX}	Receiver Downconverters Supply Voltage
47	ANTSEL	Antenna Selection Logic Input. See Table 1 for operation
48	RXTX	Rx/Tx Mode Control Logic Input. See Table 32 for operating modes.
—	EP	Exposed Paddle. Connect to the ground plane with multiple vias for proper operation and heat dissipation. Do not share with any other pin grounds and bypass capacitors' ground.

Detailed Description

The MAX2830 single-chip, low-power, direct conversion, zero-IF transceiver is designed to support 802.11g/b applications operating in the 2.4GHz to 2.5GHz band. The fully integrated transceivers include a receive path, transmit path, VCO, sigma-delta fractional-N synthesizer, crystal oscillator, RSSI, PA power detector, temperature sensor, Rx and Tx I/Q error-detection circuitry, baseband-control interface, linear power amplifier, and an Rx/Tx antenna diversity switch. The only additional components required to implement a complete radio front-end solution are a crystal, a pair of baluns, a BPF, and a small number of passive components (RCs, no inductors required).

Rx/Tx and Antenna Diversity Switches

The MAX2830 integrates an Rx/Tx switch and an antenna diversity switch before the receiver and after the power amplifier. See Figure 1 for a block diagram of the switches. The receiver and transmitter enable pin (RXTX) and the antenna selection pin (ANTSEL) determine which ports (ANT1 or ANT2) the receiver or transmitter is connected to. See Table 1 for the Rx/Tx and antenna diversity switches truth table. When RXTX = 0 (receive mode) and ANTSEL = 0, the switch provides a low-insertion loss path (main) between the ANT1 port (pins 4 and 5) and the receiver. When RXTX = 0 (receive mode) and ANTSEL = 1, the switch provides

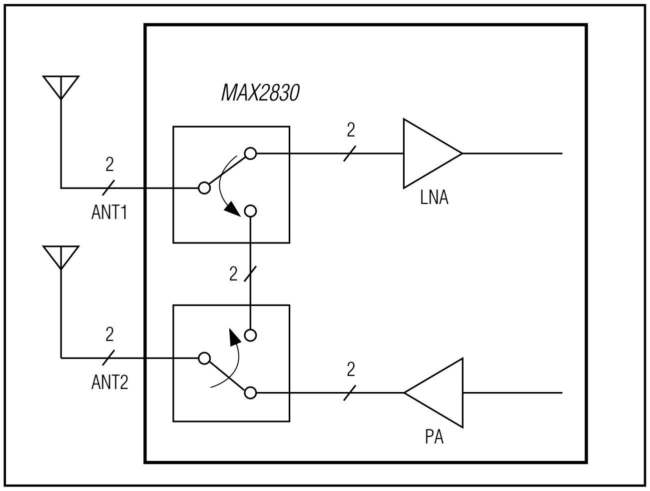


Figure 1. Simplified Rx/Tx and Antenna Diversity Switch Structure

Table 1. Rx/Tx and Antenna Diversity Switches Operation

RXTX	ANTSEL	MODE	ANTENNA
0	0	Rx (main)	Ant1_
0	1	Rx (diversity)	Ant2_
1	X	Tx	Ant2_

an antenna diversity path between the ANT2 port (pins 9 and 10) and the receiver. When RXTX = 1, the PA and transmit path are automatically connected to the ANT2 port, regardless of the logic state of ANTSEL. For solutions not requiring antenna diversity, set ANTSEL logic-level high, enabling only the ANT2 port for both receive and transmit modes.

The ANT1 and ANT2 differential ports are internally AC-coupled and internally matched to 100Ω. Directly connect 2:1 baluns or balanced bandpass filters (BPFs) to these ports for applications requiring antenna diversity. For applications not requiring antenna diversity, only a single balun or balanced BPF is required on the ANT2 port, and the ANT1 port can be left open. Provide electrically symmetrical input traces to the baluns to maintain IP2 and RF common-mode noise rejection for the receiver, and to maintain a balanced load for the PA.

Receiver

After the switch, the receiver integrates an LNA and VGA with a 95dB digitally programmable gain control range, direct-conversion downconverters, I/Q baseband lowpass filters with programmable LPF corner frequencies, analog RSSI and integrated DC-offset correction circuitry. A logic-low on the RXTX input (pin 48) and a logic-high on the $\overline{SHDN}$ input (pin 12) enable the receiver.

LNA Gain Control

The LNA has three gain modes: max gain, max gain -16dB, and max gain -33dB. The three LNA gain modes can be serially programmed through the SPI™ interface by programming bits D6:D5 in Register 11 (A3:A0 = 1011) or programmed in parallel through the digital logic gain-control pins, B7 (pin 6) and B6 (pin 3). Set bit D12 = 1 in Register 8 (A3:A0 = 1000) to enable programming through the SPI interface, or set bit D12 = 0 to enable parallel programming. See Table 2 for LNA gain-control settings.

Baseband Variable-Gain Amplifier

The receiver baseband variable-gain amplifiers provide 62dB of gain control range programmable in 2dB steps. The VGA gain can be serially programmed through the SPI interface by setting bits D4:D0 in Register 11 (A3:A0 = 1011) or programmed in parallel through the digital logic gain-control pins, B5 (pin 14), B4 (pin 34), B3 (pin 8), B2 (pin 11), and B1 (pin 23). Set bit D12 = 1 in Register 8 (A3:A0 = 1000) to enable serial programming through the serial interface or set bit D12 = 0 to enable parallel programming through the external logic pins. See Table 3 for the gain-step value and Table 4 for baseband VGA gain-control settings.

Receiver Baseband Lowpass Filter

The receiver integrates lowpass filters that provide an upper -3dB corner frequency of 8.5MHz (nominal mode) with 50dB of attenuation at 20MHz, and 45ns of group delay ripple in the passband (10kHz to 8.5MHz). The upper -3dB corner frequency is tightly controlled on-chip and does not require user adjustment. However, provisions are made to allow fine tuning of the upper -3dB

Table 2. LNA Gain-Control Settings (Pins B7:B6 or Register A3:A0 = 1011, D6:D5)

B7 OR D6	B6 OR D5	NAME	DESCRIPTION
1	1	High	Max gain
1	0	Medium	Max gain - 16dB (typ)
0	X	Low	Max gain - 33dB (typ)

Table 3. Receiver Baseband VGA Gain-Step Value (Pins B5:B1 or Register D4:D0, A3:A0 = 1011)

PIN/BIT	GAIN STEP (dB)
B1/D0	2
B2/D1	4
B3/D2	8
B4/D3	16
B5/D4	32

SPI is a trademark of Motorola, Inc.

Table 4. Baseband VGA Gain-Control Settings in Receiver Gain-Control Register (Pin B5:B1 or Register D4:D0, A3:A0 = 1011)

B5:B1 OR D4:D0	GAIN
11111	Max
11110	Max - 2dB
11101	Max - 4dB
:	:
00000	Min

Table 5. Receiver LPF Coarse -3dB Corner Frequency Settings in Register (A3:A0 = 1000)

BITS (D1:D0)	-3dB CORNER FREQUENCY (MHz)	MODE
00	7.5	11b
01	8.5	11g
10	15	Turbo 1
11	18	Turbo 2

corner frequency. In addition, coarse frequency tuning allows the -3dB corner frequency to be set to 7.5MHz (11b mode), 8.5MHz (11g mode), 15MHz (turbo 1 mode), and 18MHz (turbo 2 mode) by programming bits D1:D0 in Register 8 (A3:A0 = 1000). See Table 3. The coarse corner frequency can be fine-tuned approximately ±10% in 5% steps by programming bits D2:D0 in Register 7 (A3:A0 = 0111). See Table 6 for receiver LPF fine -3dB corner frequency adjustment.

Baseband Highpass Filter and DC Offset Correction

The receiver implements programmable AC and near-DC coupling of I/Q baseband signals. Temporary AC-coupling is used to quickly remove LO leakage and other DC offsets that could saturate the receiver outputs. When DC offsets have settled, near DC-coupling is enabled to avoid attenuation of the received signal. AC-coupling is set (-3dB highpass corner frequency of 600kHz) when a logic-high is applied to RXHP (pin 40). Near DC-coupling is set (-3dB highpass corner frequency of 100Hz nominal) when a logic-low is applied to RXHP. Bits D13:D12 in Register 7 (A3:A0 = 0111) allow the near DC-coupling -3B highpass corner frequency to be set to 100Hz (D13:D12 = 00), 4kHz (D13:D12 = X1), or 30kHz (D13:D12 = 10). See Table 7.

Table 6. Receiver LPF Fine -3dB Corner Frequency Adjustment in Register (A3:A0 = 0111)

BITS (D2:D0)	% ADJUSTMENT RELATIVE TO COARSE SETTING
000	90
001	95
010	100
011	105
100	110

Table 7. Receiver Highpass Filter -3dB Corner Frequency Programming

RXHP	A3:A0 = 0111, D13:D12	-3dB HIGHPASS CORNER FREQUENCY (Hz)
1	XX	600k
0	00	100 (recommended)
0	X1	4k
0	10	30k

X = Don't care.

Receiver I/Q Baseband Outputs

The differential outputs (RXBBI+, RXBBI-, RXBBQ+, RXBBQ-) of the baseband amplifiers have a differential output impedance of ~300Ω, and are capable of driving differential loads up to 10kΩ || 10pF. The outputs are internally biased to a common-mode voltage of 1.2V and are intended to be DC-coupled to the in-phase (I) and quadrature (Q) analog-to-digital data converter inputs of the accompanying baseband IC. Additionally, the common-mode output voltage can be adjusted from 1.2V to 1.5V through programming bits D11:D10 in Register 15 (A3:A0 = 1111).

Received Signal-Strength Indicator (RSSI)

The RSSI output (pin 16) can be programmed to multiplex an analog output voltage proportional to the received signal strength, the PA output power, or the die temperature. Set bits D9:D8 = 00 in Register 8 (A3:A0 = 1000) to enable the RSSI output in receive mode (off in transmit mode). Set bit D10 = 1 to enable the RSSI output when RXHP = 1, and disable the RSSI output when RXHP = 0. Set bit D10 = 0 to enable the RSSI output independent of RXHP. See Table 8 for a summary of the RSSI output vs. register programming and RXHP.

The RSSI provides an analog voltage proportional to the log of the sum of the squares of the I and Q channels, measured after the receive baseband filters and before the variable-gain amplifiers. The RSSI analog output voltage is proportional to the RF input signal level and LNA gain state over a 60dB range, and is not dependent upon VGA gain. See the Rx RSSI Output vs. Input Power graph in the *Typical Operating Characteristics* for further details.

Table 8. RSSI Pin Truth Table

INPUT CONDITIONS			RSSI OUTPUT
A3:A0 = 1000, D9:D8	A3:A0 = 1000, D10	RXHP	
X	0	0	No signal
00	0	1	RSSI
01	0	1	Temperature sensor
10	0	1	Power detector
00	1	X	RSSI
01	1	X	Temperature sensor
10	1	X	Power detector

X = Don't care.

Transmitter

The transmitter integrates baseband lowpass filters, direct-upconversion mixers, a VGA, a PA driver, and a linear RF PA with a power detector. A logic-high on the RXTX input (pin 48) and a logic-high on the $\overline{\text{SHDN}}$ input (pin 12) enable the transmitter. The PA outputs are routed to ANT2, regardless of the state at ANTSEL.

Transmitter I/Q Baseband Inputs

The differential analog inputs of the transmitter baseband amplifier I/Q inputs (TXBBI+, TXBBI-, TXBBQ+, TXBBQ-) have a differential impedance of 20kΩ ll 1pF. The inputs require an input common-mode voltage of 0.9V to 1.3V, which is provided by the DC-coupled I and Q DAC outputs of the accompanying baseband IC.

Transmitter Baseband Lowpass Filtering

The transmitter integrates lowpass filters that can be tuned to -3dB corner frequencies of 8MHz (11b), 11MHz (11g), 16.5MHz (turbo 1 mode), and 22.5MHz (turbo 2 mode) through programming bits D1:D0 in Register 8 (A3:A0 = 1000) and bit D5:D3 in Register 7 (A3:A0 = 0111). The -3dB corner frequency is tightly controlled on-chip and does not require user adjustment. Additionally, provisions are made to fine tune the -3dB corner frequency through bits D5:D3 in the Filter Programming register (A3:A0 = 0111). See Tables 9 and 10.

Transmitter Variable-Gain Amplifier

The variable-gain amplifier of the transmitter provides 31dB of gain control range programmable in 0.5dB steps over the top 8dB of the gain control range and in 1dB steps below that. The transmitter gain can be programmed serially through the SPI interface by setting bits D5:D0 in Register 12 (A3:A0 = 1100) or in parallel through the digital logic gain-control pins B6:B1 (pins 3, 6, 8, 11, 14, 23, and 34, respectively). Set bit D10 = 0 in Register 9 (A3:A0 = 1001) to enable parallel programming, and set bit D10 = 1 to enable programming through the 3-wire serial interface. See Table 11 for the transmitter VGA gain-control settings.

Table 9. Transmitter LPF Coarse -3dB Corner Frequency Settings in Register (A3:A0 = 1000)

BITS (D1:D0)	-3dB CORNER FREQUENCY (MHz)	MODE
00	8	11b
01	11	11g
10	16.5	Turbo 1
11	22.5	Turbo 2

Table 10. Transmitter LPF Fine -3dB Corner Frequency Adjustment in Register (A3:A0 = 0111)

BITS (D5:D3)	% ADJUSTMENT RELATIVE TO COARSE SETTING
000	90
001	95
010	100
011	105
100	110 (11g)
101	115
101–111	Not used

Table 11. Transmitter VGA Gain-Control Settings

NO.	D5:D0 OR B6:B1	OUTPUT SIGNAL POWER
63	111111	Max
62	111110	Max - 0.5dB
61	111101	Max - 1.0dB
:	:	:
49	110001	Max - 7dB
48	110000	Max - 7.5dB
47	101111	Max - 8dB
46	101110	Max - 8dB
45	101101	Max - 9dB
44	101100	Max - 9dB
:	:	:
5	000101	Max - 29dB
4	000100	Max - 29dB
3	000011	Max - 30dB
2	000010	Max - 30dB
1	000001	Max - 31dB
0	000000	Max - 31dB

Power-Amplifier Bias and Enable Delay

The MAX2830 integrates a 2-stage PA, providing +17.1dBm of output power at 5.6% error vector magnitude (EVM) (54Mbps OFDM signal) in 802.11g mode while exceeding the 802.11g spectral mask requirements. The first and second stage PA bias currents are set through programming bits D2:D0 and bits D6:D3 in Register 10 (A3:A0 = 1010), respectively. An adjustable PA enable delay, relative to the transmitter enable (RXTX low-to-high transition), can be set from 200ns to 7µs through programming bits D13:D10 in Register 10 (A3:A0 = 1010).

Power Detector

The MAX2830 integrates a voltage-peak detector at the PA output and before the switch to provide an analog voltage proportional to PA output power. See the Power Detector over Frequency and Power Detector over Supply Voltage graphs in the *Typical Operating Characteristics*. Set bits D9:D8 = 10 in Register 8 (A3:A0 = 1000) to multiplex the power-detector analog output voltage to the RSSI output (pin 16).

Synthesizer Programming

The MAX2830 integrates a 20-bit sigma-delta fractional-N synthesizer, allowing the device to achieve excellent phase-noise performance (0.9° RMS from 10kHz to 10MHz), fast PLL settling times, and an RF frequency step-size of 20Hz. The synthesizer includes a divide-by-1 or a divide-by-2 reference frequency divider, an 8-bit integer portion main divider with a divisor range programmable from 64 to 255, and a 20-bit fractional portion main-divider. Bit D2 in Register 5 (A3:A0 = 0101) sets the reference oscillator divider ratio to 1 or 2. Bits D7:D0 in Register 3 (A3:A0 = 0011) set the integer portion of the main divider. The 20-bit fractional portion of the main-divider is split between two registers. The 14 MSBs of the fractional portion are set in Register 4 (A3:A0 = 0100), and the 6 LSBs of the fractional portion of the main divider are set in Register 3 (A3:A0 = 0011). See Tables 12 and 13.

Calculating Integer and Fractional Divider Ratios

The desired integer and fractional divider ratios can be calculated by dividing the RF frequency (f_{RF}) by f_{COMP}. For nominal 802.11g/b operation, a 40MHz reference oscillator is divided by 2 to generate a 20MHz comparison frequency (f_{COMP}). The following method can be used when calculating divider ratios supporting various reference and comparison frequencies:

LO Frequency Divider = f_{RF} / f_{COMP} = 2437MHz / 20MHz = 121.85

Integer Divider = 121 (d) = 0111 1001 (binary)

Fractional Divider = 0.85 x (2^{20} - 1) = 891289 (decimal) = 1101 1001 1001 1001 1001

See Table 14 for integer and fractional divider ratios for 802.11g/b systems using a 20MHz comparison frequency.

Table 12. Integer Divider Register (A3:A0 = 0011)

BIT	RECOMMENDED	DESCRIPTION
D13:D8	000000	6 LSBs of 20-Bit Fractional Portion of Main Divider
D7:D0	01111001	8-Bit Integer Portion of Main Divider. Programmable from 64 to 255.

Table 13. Fractional Divider Register (A3:A0 = 0100)

BIT	RECOMMENDED	DESCRIPTION
D13:D0	11011001100110	14 MSBs of 20-Bit Fractional Portion of Main Divider

Table 14. IEEE 802.11g/b Divider-Ratio Programming Words

f_{RF} (MHz)	(f_{RF} / f_{COMP})	INTEGER DIVIDER	FRACTIONAL DIVIDER	
		A3:A0 = 0011, D7:D0	A3:A0 = 0100, D13:D0	A3:A0 = 0011, D13:D8
2412	120.6	0111 1000b	2666h	1Ah
2417	120.85	0111 1000b	3666h	1Ah
2422	121.1	0111 1001b	0666h	1Ah
2427	121.35	0111 1001b	1666h	1Ah
2432	121.6	0111 1001b	2666h	1Ah
2437	121.85	0111 1001b	3666h	1Ah
2442	122.1	0111 1010b	0666h	1Ah
2447	122.35	0111 1010b	1666h	1Ah
2452	122.6	0111 1010b	2666h	1Ah
2457	122.85	0111 1010b	3666h	1Ah
2462	123.1	0111 1011b	0666h	1Ah
2467	123.35	0111 1011b	1666h	1Ah
2472	123.6	0111 1011b	2666h	1Ah
2484	124.2	0111 1100b	0CCCh	33h

Crystal Oscillator

The crystal oscillator has been optimized to work with low-cost crystals (e.g., Kyocera CX-3225SB). See Figure 2. The crystal oscillator frequency can be fine tuned through bits D6:D0 in Register 14 (A3:A0 = 1110), which control the value of C_{TUNE} from 0.5pF to 15.4pF in 0.12pF steps. See the Crystal-Oscillator Offset Frequency vs. Crystal-Oscillator Tuning Bits graph in the *Typical Operating Characteristics*. The crystal oscillator can be used as a buffer for an external reference frequency source. In this case, the reference signal is AC-coupled to the XTAL pin, and capacitors C1 and C2 are not connected. When used as a buffer, the XTAL input pin has to be AC-coupled. The XTAL pin has an input impedance of 5kΩ II 4pF, (set D6:D0 = 0000000 in Register 14 A3:A0 = 1110).

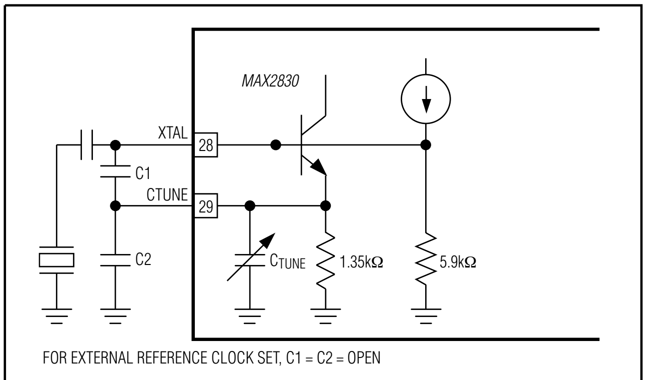


Figure 2. Crystal Oscillator Schematic

Reference Clock Output Divider/Buffer

The reference oscillator of the MAX2830 has a divider and a buffered output for routing the reference clock to the accompanying baseband IC. Bit D10 in Register 14 (A3:A0 = 1110) sets the buffer divider to divide by 1 or 2, independent of the divide ratio for the reference frequency provided to the PLL. Bit B9 in the same register enables or disables the reference buffer output. See the Clock Output waveform in the *Typical Operating Characteristics*.

Loop Filter

The PLL charge-pump output, CPOUT (pin 24), connects to an external third-order, lowpass RC loop-filter, which in turn connects to the voltage tuning input, TUNE (pin 32), of the VCO, completing the PLL loop. The charge-pump output sink and source current is 1mA, and the VCO tuning gain is 103MHz/V at 0.5V tune voltage and 86MHz/V at 2.2V tune voltage. The RC loop-filter values have been optimized for a loop bandwidth of 150kHz, to achieve the desired Rx/Tx turnaround settling time, while maintaining loop stability and good phase noise. Refer to the MAX2830 EV kit schematic for the recommended loop-filter component values. Keep the line from this pin to the tune input as short as possible to prevent spurious pickup.

Lock-Detector Output

The PLL features a logic lock-detect output. A logic-high indicates the PLL is locked, and a logic-low indicates the PLL is not locked. Bit D5 in Register 5 (A3:A0 = 0101) enables or disables the lock-detect output. Bit

D12 in Register 1 (A3:A0 = 0001) configures the lock-detect output as a CMOS or open-drain output. In open-drain output mode, bit D9 in Register 5 (A3:A0 = 0101) enables or disables an internal 30kΩ pullup resistor from the open-drain output.

Programmable Registers and 3-Wire SPI-Interface

The MAX2830 includes 16 programmable, 18-bit registers. The 14 most significant bits (MSBs) are used for register data. The 4 least significant bits (LSBs) of each register contain the register address. See Table 15 for a summary of the registers and recommended register settings.

Register data is loaded through the 3-wire SPI/MICROWIRE™-compatible serial interface. Data is shifted in MSB first and is framed by $\overline{CS}$. When $\overline{CS}$ is low, the clock is active, and data is shifted with the rising edge of the clock. When $\overline{CS}$ transitions high, the shift register is latched into the register selected by the contents of the address bits. See Figure 3. Only the last 18 bits shifted into the device are retained in the shift register. No check is made on the number of clock pulses. For programming data words less than 14 bits long, only the required data bits and the address bits need to be shifted, resulting in faster Rx and Tx gain control where only the LSBs need to be programmed.

Table 15. Recommended Register Settings*

REGISTER	DATA														ADDRESS	TABLE
	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	(A3:A0)	
0	0	1	0	1	1	1	0	1	0	0	0	0	0	0	0000	15
1	0	1	0	0	0	1	1	0	0	1	1	0	1	0	0001	16
2	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0010	17
3	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0011	18
4	1	1	0	1	1	0	0	1	1	0	0	1	1	0	0100	19
5	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0101	20
6	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0110	21
7	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0111	22
8	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1000	23
9	0	0	0	0	1	1	1	0	1	1	0	1	0	1	1001	24
10	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1010	25
11	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1011	26
12	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1100	27
13	0	0	1	1	1	0	1	0	0	1	0	0	1	0	1101	28
14	0	0	0	0	1	1	0	0	1	1	1	0	1	1	1110	29
15	0	0	0	0	0	1	0	1	0	0	0	1	0	1	1111	30

**The power-on register settings are not production tested. Recommended register settings must be loaded after V_{CC} is supplied.*

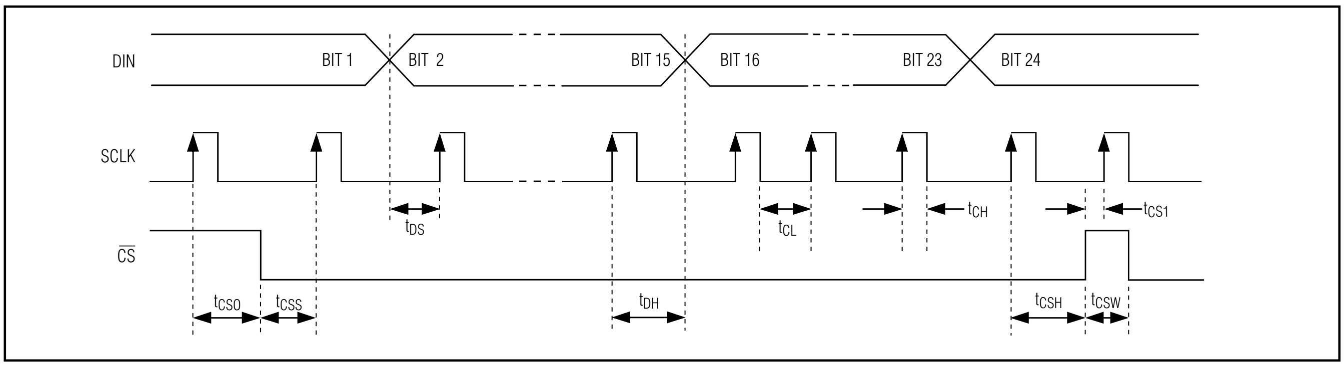


Figure 3. 3-Wire SPI Serial-Interface Timing Diagram

MICROWIRE is a trademark of National Semiconductor Corp.

Table 16. Register 0 (A3:A0 = 0000)

DATA BITS	RECOMMENDED	DESCRIPTION
D13:D11	000	Set to recommended value.
D10	1	Fractional-N PLL Mode Enable. Set 1 to enable the fractional-N PLL or set 0 to enable the integer-N PLL.
D9:D0	1101000000	Set to recommended value.

Table 17. Register 1 (A3:A0 = 0001)

DATA BITS	RECOMMENDED	DESCRIPTION
D13	0	Set to recommended value.
D12	1	Lock-Detector Output Select. Set to 1 for CMOS Output. Set to 0 for open-drain output. Bit D9 in register (A3:A0 = 0101) enables or disables an internal 30kΩ pullup resistor in open-drain output mode.
D11:D0	000110011010	Set to recommended value.

Table 18. Register 2 (A3:A0 = 0010)

DATA BITS	RECOMMENDED	DESCRIPTION
D13:D0	01000000000011	Set to recommended value.

This register contains the 8-bit integer portion and 6 LSBs of the fractional portion of the divider ratio of the synthesizer.

Table 19. Register 3 (A3:A0 = 0011)

BIT	RECOMMENDED	DESCRIPTION
D13:D8	00000	6 LSBs of 20-Bit Fractional Portion of Main Divider
D7:D0	01111001	8-Bit Integer Portion of Main Divider. Programmable from 64 to 255.

Table 20. Register 4 (A3:A0 = 0100)

BIT	RECOMMENDED	DESCRIPTION
D13:D0	11011001100110	14 MSBs of 20-Bit Fractional Portion of Main Divider

Table 21. Register 5 (A3:A0 = 0101)

BIT	RECOMMENDED	DESCRIPTION
D13:D10	0000	Set to recommended value.
D9	0	Lock-Detect Output Internal Pullup Resistor Enable. Set to 1 to enable internal 30kΩ pullup resistor or set to 0 to disable the resistor. Only available when lock-detect, open-drain output is selected (A3:A0 = 0001, D12 = 1).
D8:D6	010	Set to recommended value.
D5	1	Lock-Detect Output Enable. Set to 1 to enable the lock-detect output or set to 0 to disable the output. The output is high impedance when disabled.
D4:D3	00	Set to recommended value.
D2	1	Reference Frequency Divider Ratio to PLL. Set to 0 to divide by 1. Set to 1 to divide by 2.
D1:D0	00	Set to recommended value.

Table 22. Register 6 (A3:A0 = 0110)

DATA BIT	RECOMMENDED	DESCRIPTION
D13	0	Set to recommended value.
D12:D11	00	Tx I/Q Calibration LO Leakage and Sideband Detector Gain-Control Bits. D12:D11 = 00: 9dB; 01 19dB; 10: 29dB; 11: 39dB.
D10:D7	0000	Set to recommended value.
D6	1	Power-Detector Enable in Tx Mode. Set to 1 to enable the power detector or set to 0 to disable the detector.
D5:D2	1000	Set to recommended value.
D1	0	Tx Calibration Mode. Set to 1 to place the device in Tx calibration mode or 0 to place the device in normal Tx mode when RXTX is set to 1 (see Table 32).
D0	0	Rx Calibration Mode. Set to 1 to place the device in Rx calibration mode or 0 to place the device in normal Rx mode when RXTX is set to 0 (see Table 32).

Table 23. Register 7 (A3:A0 = 0111)

BIT	RECOMMENDED	DESCRIPTION
D13:D12	01	Receiver Highpass Corner Frequency Setting for RXHP = 0. Set to 00 for 100Hz, X1 for 4kHz, and 10 for 30kHz.
D11:D6	000000	Set to recommended value.
D5:D3	100	Transmitter Lowpass Filter Corner Frequency Fine Adjustment (Relative to Coarse Setting). See Table 9. Bits D1:D0 in A3:A0 = 1000 provide the lowpass filter corner coarse adjustment.
D2:D0	010	Receiver Lowpass Filter Corner Frequency Fine Adjustment (Relative to Coarse Setting). See Table 6. Bits D1:D0 in A3:A0 = 1000 provide the lowpass filter corner coarse adjustment.

Table 24. Register 8 (A3:A0 = 1000)

BIT	RECOMMENDED	DESCRIPTION
D13	1	Set to recommended value.
D12	0	Enable Receiver Gain Programming Through the Serial Interface. Set to 1 to enable programming through the 3-wire serial interface (D6:D0 in Register A3:A0 = 1011). Set to 0 to enable programming in parallel through external digital pins (B7:B1).
D11	0	Set to recommended value.
D10	0	RSSI Operating Mode. Set to 1 to enable RSSI output independent of RXHP. Set to 0 to disable RSSI output if RXHP = 0, and enable the RSSI output if RXHP = 1.
D9:D8	00	RSSI, Power Detector, or Temperature Sensor Output Select. Set to 00 to enable the RSSI output in receive mode. Set to 01 to enable the temperature sensor output in receive and transmit modes. Set to 10 to enable the power-detector output in transmit mode. See Table 7.
D7:D2	001000	Set to recommended value.
D1:D0	01	Receiver and Transmitter Lowpass Filter Corner Frequency Coarse Adjustment. See Tables 4 and 7.

Table 25. Register 9 (A3:A0 = 1001)

BIT	RECOMMENDED	DESCRIPTION
D13:D11	000	Set to recommended value.
D10	0	Enable Transmitter Gain Programming Through the Serial or Parallel Interface. Set to 1 to enable programming through the 3-wire serial interface (D5:D0 in Register A3:A0 = 1011). Set to 0 to enable programming in parallel through external digital pins (B6:B1).
D9:D0	1110110101	Set to recommended value.

Table 26. Register 10 (A3:A0 = 1010)

BIT	RECOMMENDED	DESCRIPTION
D13:D10	0111	Power-Amplifier Enable Delay. Sets a delay between RXTX low-to-high transition and internal PA enable. Programmable in 0.5µs steps. D13:D10 = 0001 (0.2µs) and D13:D10 = 1111 (7µs).
D9:D7	011	Set to recommended value.
D6:D3	0100	Second-Stage Power-Amplifier Bias Current Adjustment. Set to XXXX for 802.11g/b.
D2:D0	100	First-Stage Power-Amplifier Bias Current Adjustment. Set to XXX for 802.11g/b.

Table 27. Register 11 (A3:A0 = 1011)

BIT	RECOMMENDED	DESCRIPTION
D13:D7	0000000	Set to recommended value.
D6:D5	11	LNA Gain Control. Set to 11 for high-gain mode. Set to 10 for medium-gain mode, reducing LNA gain by 16dB. Set to 0X for low-gain mode, reducing LNA gain by 33dB.
D4:D0	11111	Receiver VGA Control. Set D4:D0 = 00000 for minimum gain and D4:D0 = 11111 for maximum gain.

Table 28. Register 12 (A3:A0 = 1100)

BIT	RECOMMENDED	DESCRIPTION
D13:D6	00000101	Set to recommended value.
D5:D0	000000	Transmitter VGA Gain Control. Set D5:D0 = 000000 for minimum gain, and set D5:D0 = 111111 for maximum gain.

Table 29. Register 13 (A3:A0 = 1101)

BIT	RECOMMENDED	DESCRIPTION
D13:D10	0011	Set to recommended value.
D9:D6	1010	Set to recommended value.
D5:D0	010010	Set to recommended value.

Table 30. Register 14 (A3:A0 = 1110)

BIT	RECOMMENDED	DESCRIPTION
D13:D11	000	Set to recommended value.
D10	0	Reference Clock Output Divider Ratio. Set 1 to divide by 2 or set 0 to divide by 1.
D9	1	Reference Clock Output Enable. Set 1 to enable the reference clock output or set 0 to disable.
D8:D7	10	Set to recommended value.
D6:D0	XXXXXXX	Crystal-Oscillator Fine Tune. Tunes crystal oscillator over ±20ppm to within ±1ppm.

X = Don't care.

Table 31. Register 15 (A3:A0 = 1111)

BIT	RECOMMENDED	DESCRIPTION
D13:D12	00	Set to recommended value.
D11:D10	00	Receiver I/Q Output Common-Mode Voltage Adjustment. Set D11:D10 = 00: 1.1V, 01: 1.2V, 10: 1.3V, 11: 1.45V.
D9:D0	0101000101	Set to recommended value.

Table 32. Operating Mode Table

MODE	LOGIC PINS		REGISTER SETTINGS	CIRCUIT BLOCK STATES			
	$\overline{\text{SHDN}}$	RXTX	D1:D0 (A3:A0 = 0110)	Rx PATH	Tx PATH	PLL, VCO, LO GEN, AUTOTUNER	CALIBRATION SECTIONS ON
Shutdown	0	0	00	Off	Off	Off	None
Standby	0	1	00	Off	Off	On	None
Rx	1	0	X0	On	Off	On	None
Tx	1	1	0X	Off	On	On	None
Rx Calibration	1	0	X1	On (except LNA)	Upconverters	On	Cal tone, RF phase shift, Tx filter
Tx Calibration	1	1	1X	Off	On (except PA driver and PA)	On	AM detector, Rx I/Q buffers

X = Don't care.
Note: *See Table 1 for Rx/Tx and antenna diversity operating mode.*

Modes of Operation

The modes of operation for the MAX2830 are shutdown, standby, transmit, receive, transmitter calibration, and receiver calibration. See Table 32 for a summary of the modes of operation. The logic-input pins, $\overline{\text{SHDN}}$ (pin 12) and RXTX (pin 48), control the various modes.

Shutdown Mode

The MAX2830 features a low-power shutdown mode that disables all circuit blocks, except the serial-interface and internal registers, allowing the registers to be loaded and values maintained, as long as V_{CC} is applied. Set $\overline{\text{SHDN}}$ and RXTX logic-low to place the device in shutdown mode. After a supply voltage ramp up, supply current in shutdown mode could be high. Program the default value to SPI register 0 to eliminate high shutdown current.

Standby Mode

The standby mode is used to enable the frequency synthesizer block while the rest of the device is powered down. In this mode, the PLL, VCO, and LO generators are on, so that Tx or Rx modes can be quickly enabled from this mode. Set $\overline{SHDN}$ to a logic-low and RXTX to a logic-high to place the device in standby mode.

Receive (Rx) Mode

The complete receive signal path is enabled in this mode. Set $\overline{SHDN}$ to logic-high and RXTX to logic-low to place the device in Rx mode.

Transmit (Tx) Mode

The complete transmitter signal path is enabled in this mode. Set $\overline{SHDN}$ and RXTX to logic-high to place the device in Tx mode.

Rx/Tx Calibration Mode

The MAX2830 features Rx/Tx calibration modes to detect I/Q imbalances and transmit LO leakage. In the Tx calibration mode, all Tx circuit blocks, except the PA driver and external PA, are powered on and active. The AM detector and receiver I and Q channel buffers are also on, along with multiplexers in the receiver side to route this AM detector's signal. In this mode, the LO leakage calibration is done only for the LO leakage signal that is present at the center frequency of the channel (i.e., in the middle of the OFDM or QPSK spectrum). The LO leakage calibration includes the effect of all DC offsets in the entire baseband paths of the I/Q modulator and direct leakage of the LO to the I/Q modulator output.

The LO leakage and sideband detector output are taken at the receiver I and Q channel outputs during this calibration phase.

During Tx LO leakage and I/Q imbalance calibration, a sine and cosine signal ($f = f_{TONE}$) is input to the baseband I/Q Tx pins from the baseband IC. At the LO leakage and sideband-detector output, the LO leakage corresponds to the signal at f_{TONE} and the sideband suppression corresponds to the signal at 2 x f_{TONE}. The output power of these signals vary 1dB for 1dB of variation in the LO leakage and sideband suppression. To calibrate the Tx path, first set the power-detector gain to 9dB using D12:D11 in Register 6 (see Table 22). Adjust the DC offset of the baseband inputs to minimize the signal at f_{TONE} (LO leakage). Then, adjust the baseband input relative magnitude and phase offsets to reduce the signal at 2 x f_{TONE}.

In Rx calibration mode, the calibrated Tx RF signal is internally routed to the Rx inputs. In this mode, the VCO/LO generator/PLL blocks are powered on and active except for the low-noise amplifier (LNA).

Applications Information

Layout Issues

The MAX2830 EV kit can be used as a starting point for layout. For best performance, take into consideration grounding and RF, baseband, and power-supply routing. Make connections from vias to the ground plane as short as possible. Do not connect the device ground pin to the exposed paddle ground. Keep the buffered clock output trace as short as possible. Do not share the trace with the RF input layer, especially on or interlayer or back side of the board. On the high-impedance ports, keep traces short to minimize shunt capacitance. EV kit Gerber files can be requested at www.maxim-ic.com.

Power-Supply Layout

To minimize coupling between different sections of the IC, a star power-supply routing configuration with a large decoupling capacitor at a central V_{CC} node is recommended. The V_{CC} traces branch out from this node, each going to a separate V_{CC} node in the circuit. Place a bypass capacitor as close as possible to each supply pin. This arrangement provides local decoupling at each V_{CC} pin. Use at least one via per bypass capacitor for a low-inductance ground connection. Do not share the capacitor ground vias with any other branch and the exposed paddle ground.

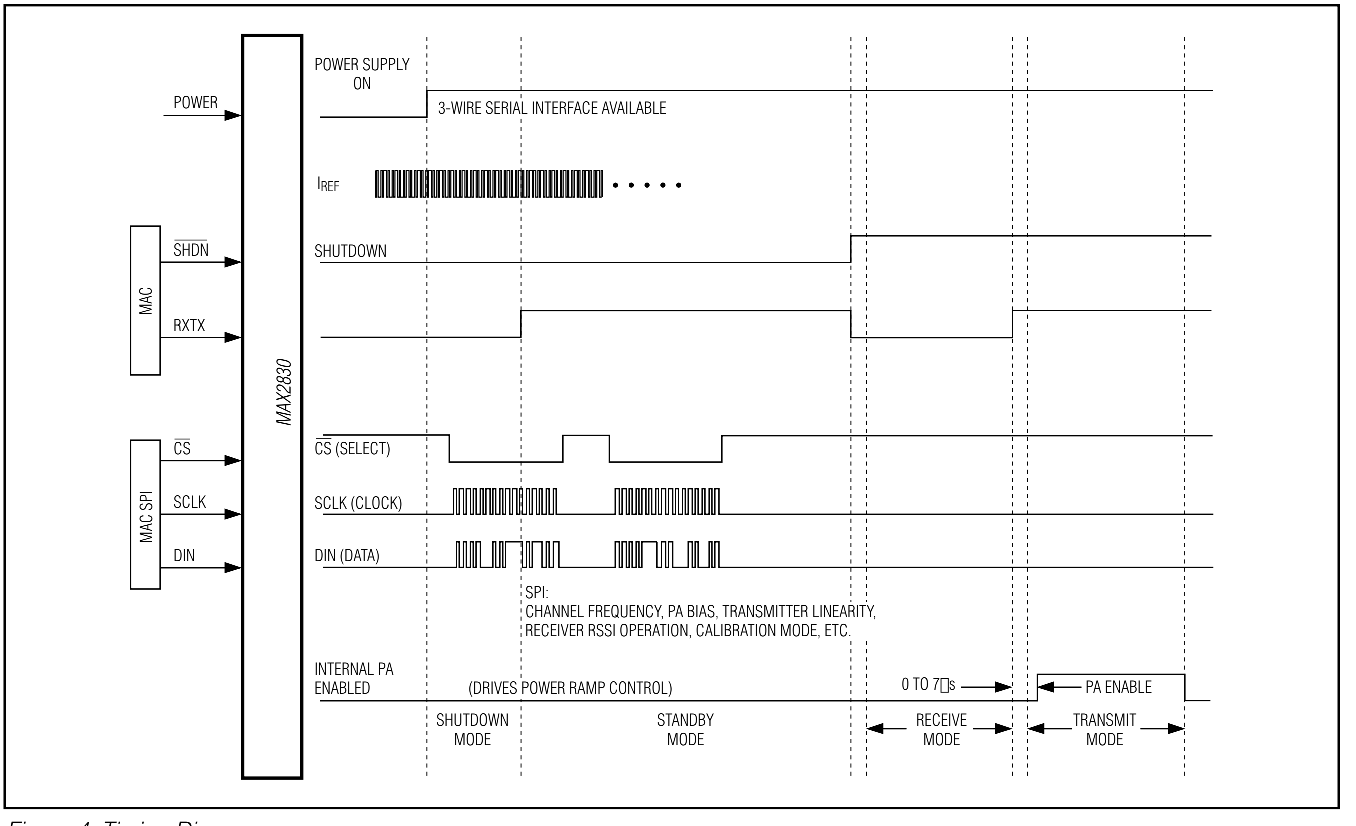
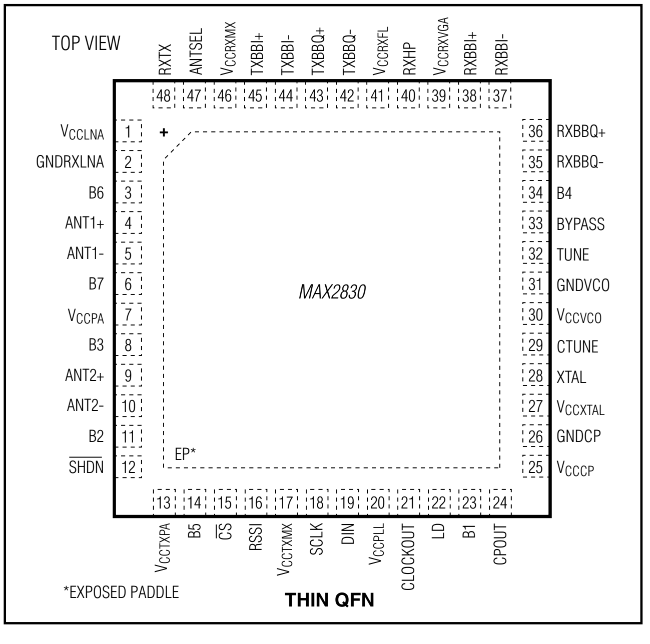


Figure 4. Timing Diagram

Pin Configuration



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFN-EP	T4877+4	21-0144	90-0130

2.4GHz to 2.5GHz 802.11g/b RF Transceiver, PA, and Rx/Tx/Antenna Diversity Switch

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/07	Initial release	—
1	7/09	Corrected Table 12	24
2	3/11	Corrected conditions for Rx I/Q Output Common-Mode Voltage Variation in the *DC Electrical Characteristics*; corrected Tables 15 and 31; added text to *Shutdown Mode* section	2, 26, 30

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