Dual nanoPower Op Amps in Tiny WLP and TDFN Packages

General Description

The MAX40018 is a dual operational amplifier that consumes only 400nA supply current (per channel). At such low power consumption, the device is ideal for battery-powered applications such as portable medical equipment, portable instruments and wireless handsets.

The MAX40018 operates from a single 1.7V to 5.5V supply, allowing the device to be powered by the same 1.8V, 2.5V, or 3.3V nominal supply that powers the microcontroller. The MAX40018 features rail-to-rail outputs and is unity-gain stable with a 9kHz gain bandwidth product (GBP).

The ultra-low supply current, ultra-low input bias current, low operating voltage, and rail-to-rail output capabilities make this dual operational amplifier ideal for use with single lithium-ion (Li+), or two-cell NiCd or alkaline batteries.

The MAX40018 is available in a tiny, 8-bump, 1.63mm x 0.91mm wafer-level package (WLP), with a bump pitch of 0.4mm, as well as in an 8-pin 3mm x 3mm TDFN package. The device is specified over the -40° C to $+125^{\circ}$ C, automotive temperature range.

Applications

- Wearable Devices
- Handheld Devices
- Notebook and Tablet Computers
- Portable Medical Devices
- Portable Instrumentation

Benefits and Features

- Ultra-Low Power Preserves Battery Life
 400nA Typical Supply Current (Per Channel)
- Single 1.7V to 5.5V Supply Voltage Range
 The Device Can be Powered From the Same 1.8V/2.5V/3.3V/5V System Rails
- Tiny Packages Save Board Space
 - 1.63mm x 0.91mm x 0.5mm WLP-8 with 0.4mm Bump Pitch
 - 3mm x 3mm x 0.75mm TDFN-8 Package
- Precision Specifications for Buffer/Filter/Gain Stages
 - Low 350µV Input Offset Voltage
 - Rail-to-Rail Output Voltage
 - 9kHz GBP
 - Low 0.1pA Input Bias Current
 - Unity-Gain Stable
- -40°C to +125°C Temperature Range

Ordering Information appears at end of data sheet.

Simplified Block Diagram





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Absolute Maximum Ratings

V _{DD} to V _{SS} 0.3	3V to +6V
OUT_ to V_{SS} - 0.3V to V_{I}	+ 0.3V + _{OC}
IN_+, IN to V _{SS} V _{SS} - 0.3V to V _I	+ 0.3V + _{OC}
IN_+ to IN	±2V
Continuous Current Into Any Input Pin	±10mA
Continuous Current Into Any Output Pin	±20mA
Output Short-Circuit Duration to V _{DD} or V _{SS}	10s
Continuous Power Dissipation (T _A = +70°C; 8-Bump \	NLP,
derate 11.4mW/°C above +70°C)	912mW

Continuous Power Dissipation ($T_A = +70^{\circ}C$; TI	DFN-8,
derate 24.4mW/°C above +70°C)	1951.2mW
Operating Temperature Range	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Reflow Soldering Peak Temperature (Pb-free)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TDFN-8

PACKAGE CODE	T833+2
Outline Number	<u>21-0137</u>
Land Pattern Number	90-0059
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	8°C/W

WLP-8

PACKAGE CODE	N80B1+1
Outline Number	21-100228
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	87.71°C/W
Junction to Case (θ _{JC})	N/A

For the latest package outline information and land patterns (footprints), go to <u>www.maximintegrated.com/packages</u>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to <u>www.maximintegrated.com/thermal-tutorial</u>.

Electrical Characteristics

 $(V_{DD} = +3V, V_{SS} = 0V, V_{CM} = 0.5V, V_{OUT} = V_{DD}/2, R_L = 1M\Omega$ to $V_{DD}/2, T_A = +25^{\circ}C$, unless otherwise noted (Note 1).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V _{DD}	Guaranteed by PSRR tests			5.5	V
Supply Current (Dual)	I _{DD}	T _A = +25°C		0.8	1.3	
		$T_A = -40^{\circ}C$ to $+85^{\circ}C$			1.4	μA
		$T_{A} = -40^{\circ}C \text{ to } +125^{\circ}C$			1.6	

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Electrical Characteristics (continued)

 $(V_{DD} = +3V, V_{SS} = 0V, V_{CM} = 0.5V, V_{OUT} = V_{DD}/2, R_L = 1M\Omega$ to $V_{DD}/2, T_A = +25^{\circ}C$, unless otherwise noted (Note 1).)

PARAMETER	SYMBOL	CONDITIONS		MIN	ТҮР	MAX	UNITS
		T _A = +25°C, V _{SS} - 0.1V < V _{CM} < V _{DD} - 1.1V			±0.35	±1.3	
Input Offset Voltage	V _{OS}	T _A = -40°C to +125°C, V _{SS} - 0.1V < V _{CM} < V _{DD} - 1.1V				±9	mV
Input Offset Drift					6.2	88	µV/°C
Input Pige Current (Note 2)		T _A = +25°C			0.1		n A
Input Bias Current (Note 2)	I _B	$T_A = -40^{\circ}C \text{ to } +125^{\circ}C$	C			200	рА
Input Offeet Current (Nete 2)		T _A = +25°C			0.1		54
Input Offset Current (Note 2)	los	$T_A = -40^{\circ}C \text{ to } +125^{\circ}C$	C			60	pА
Input Capacitance		Either input, over ent	ire CMVR		3		pF
Common Mode Voltage Range	CMVR	Guaranteed by CMR	R tests	V _{SS} - 0.1		V _{DD} - 1.1	V
Common Mode Dejection Datio	CMRR	DC, $(V_{SS} - 0.1V) \le V$	_{CM} ≤ (V _{DD} - 1.1V)	70	95		dD
Common Mode Rejection Ratio	CIVIRR	AC, 100mV _{PP} 1kHz,	with output at V _{DD} /2		48		dB
Dower Supply Dejection Datio		DC, 1.7V ≤ V _{DD} ≤ 5.5V		67	88		dB
Power Supply Rejection Ratio	PSRR	AC, 100mV _{PP} 1kHz, superimposed on V _{DD}			35		ав
Open Loop Gain	A _{VOL}	$R_L = 1M\Omega, V_{OUT} = +$	50mV to V _{DD} - 50mV	75	110		dB
	V _{OH}	Swing high specified as V _{DD} - V _{OUT}	$R_L = 100 k\Omega$ to $V_{DD}/2$		2.2	8	mV
Output Voltage Swing			$R_L = 10k\Omega$ to $V_{DD}/2$		19.3	70	
Output voltage Swillg	V _{OL}	Swing low specified	$R_L = 100 k\Omega$ to $V_{DD}/2$		2.2	8	
		as V _{OUT} - V _{SS}	$R_L = 10k\Omega$ to $V_{DD}/2$		20	70	
Output Short-Circuit Current		Shorted to V _{SS} (sourcing) Shorted to V _{DD} (sinking)			8		m۸
Output Short-Circuit Current					8		— mA
Gain Bandwidth Product	GBP	$A_V = 1V/V$, $C_L = 20p$	۶F		9		kHz
Phase Margin	φΜ	C _L = 20pF			64		0
Slew Rate	SR	V _{OUT} = 1V _{PP} step, A	$V_V = 1V/V$		6.4		V/ms
Settling Time		100mV step, $A_V = 1V/V$, $C_L = 20pF$, 0.1% settling			165		μs
Input Voltage Noise Density	e _N	f = 1kHz			730		nV/√Hz
Noise Voltage		From 0.1Hz to 10Hz			7		μV _{RMS}
Power-On Time	t _{ON}	Output reaches 1% of final value			0.39		ms
Stable Capacitive Load	CL	No sustained oscillations			30		pF
Crosstalk		IN1+, 100mV _{PP} , f = 1		78		dB	

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Guaranteed by design.

Dual nanoPower Op Amps in Tiny WLP and TDFN Packages

Typical Operating Characteristics

 $(V_{DD}$ = +3.0V, V_{SS} = 0V, V_{CM} = 0.5V, V_{OUT} = $V_{DD}/2$, R_L = 1M Ω to $V_{DD}/2$, T_A = +25°C, unless otherwise noted.)





INPUT OFFSET VOLTAGE vs. INPUT COMMON MODE VOLTAGE-CHANNEL B





OUTPUT VOLTAGE LOW vs. OUTPUT SINK CURRENT





INPUT OFFSET CURRENT



INPUT COMMON MODE VOLTAGE (V)



50

TEMPERATURE (°C)

100

150

INPUT BIAS CURRENT vs. INPUT COMMON MODE VOLTAGE



INPUT BIAS CURRENT (pA)

1

0.01

0

-50

Dual nanoPower Op Amps in Tiny WLP and TDFN Packages

Typical Operating Characteristics (continued)

(V_{DD} = +3.0V, V_{SS} = 0V, V_{CM} = 0.5V, V_{OUT} = V_{DD}/2, R_L = 1M Ω to V_{DD}/2, T_A = +25°C, unless otherwise noted.)













INPUT VOLTAGE NOISE DENSITY vs. FREQUENCY



Dual nanoPower Op Amps in Tiny WLP and TDFN Packages

Typical Operating Characteristics (continued)

 $(V_{DD} = +3.0V, V_{SS} = 0V, V_{CM} = 0.5V, V_{OUT} = V_{DD}/2, R_L = 1M\Omega \text{ to } V_{DD}/2, T_A = +25^{\circ}C, \text{ unless otherwise noted.})$



Dual nanoPower Op Amps in Tiny WLP and TDFN Packages

Pin Configuration





Dual nanoPower Op Amps in Tiny WLP and TDFN Packages

Pin Description

P	IN	NAME	FUNCTION	
WLP	TDFN	INAIVIE		
A1	1	OUT1	Amplifier 1 Output	
A2	2	IN1-	Inverting Input, Channel 1	
A3	3	IN1+	Noninverting Input, Channel 1	
A4	4	V _{SS}	Negative Power Supply Input. Connect V _{SS} to 0V in single-supply application.	
B1	8	V _{DD}	Positive Power Supply Input	
B2	7	OUT2	Amplifier 2 Output	
B3	6	IN2-	Inverting Input, Channel 2	
B4	5	IN2+	Noninverting Input, Channel 2	
		EP	Exposed Pad. Connect EP to V _{SS} or leave unconnected.	

Detailed Description

The MAX40018 is a dual operational amplifier that draws just 400nA supply current (typical, per channel). It is ideal for battery-powered applications, such as portable medical equipment, portable instruments, and wireless handsets. The amplifiers feature rail-to-rail outputs and are unity-gain stable with a 9kHz GBP. The ultra-low supply current, ultra-low input bias current, low operating voltage, and rail-to-rail output capabilities make this dual operational amplifier ideal for use with single lithium-ion (Li+), or two-cell NiCd or alkaline batteries.

Power Supplies and PCB Layout

The MAX40018 operates from a single +1.7V to +5.5V power supply, or dual $\pm 0.85V$ to $\pm 2.75V$ power supplies. Bypass the power supplies with a 0.1μ F ceramic capacitor placed close to V_{DD} and V_{SS} pins. Adding a solid ground plane improves performance generally by decreasing the noise at the op amp's inputs. However, in very high impedance circuits, it may be worth removing the ground plane under the IN_- pins to reduce the stray capacitance and help avoid reducing the phase margin. To further decrease stray capacitance, minimize PCB trace lengths and resistor and capacitor leads, and place external components close to the amplifier's pins.

Ground Sensing Inputs

The common-mode voltage range of the MAX40018 extends down to V_{SS} - 0.1V, and offers excellent common-mode rejection. This feature allows input voltage below ground in a single power supply application, where ground sensing is very common. This op amp is also guaranteed not to exhibit phase reversal when either input is overdriven.

Rail-To-Rail Outputs

The outputs of the MAX40018 dual op amps are guaranteed to swing within 8mV of the power supply rails with a $100k\Omega$ load.

ESD Protection

The MAX40018 input and output pins are protected against electrical discharge (ESD) with dedicated diodes as shown in the <u>Simplified Block Diagram</u>. Caution must be used when input voltages are beyond the power rails. Also, the maximum current in or out of any input pin as shown in the <u>Absolute Maximum Ratings</u> must be observed.

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Stability

The MAX40018 maintains stability in its minimum gain configuration while driving capacitive loads up to 30pF or so. Larger capacitive loading is achieved using the techniques described in the Capacitive Load Stability section below. Although this amplifier is primarily designed for low frequency applications, good layout can still be extremely important, especially if very high value resistors are being used, as is likely in ultra-low-power circuitry. However, some stray capacitance may be unavoidable; and it may be necessary to add a 2pF to 10pF capacitor across the feedback resistor, as shown in Figure 1. Select the smallest capacitor value that ensures stability so that BW and settling time are not significantly impacted.

Capacitive Load Stability

Driving large capacitive loads can cause instability in amplifiers. The MAX40018 is stable with capacitive loads up to 30pF. Stability with higher capacitive loads can be achieved by adding a resistive load in parallel with the capacitive load, as shown in Figure 2. This resistor improves the circuit's phase margin by reducing the effective bandwidth of the amplifier. The graph in the <u>Typical</u> <u>Operating Characteristics</u> gives the stable operation region for capacitive load versus resistive load.



Figure 1. Compensation for Feedback Node Capacitance



Figure 2. RL Improving Capacitive Load Drive Capability of Op Amp

Dual nanoPower Op Amps in Tiny WLP and TDFN Packages

Applications Information

Optimizing for Ultra-Low-Power Applications

The MAX40018 is designed for ultra-low-power applications. To reduce the power consumption in the application circuits, use impedance as large as the performance allows. For example, choose low leakage ceramic capacitors and high-value resistors. If moisture in high-value resistors causes stray capacitance or current leakage, use special coating process to reduce the leakage.

General Purpose Active Filters

<u>Figure 3</u> shows an active band-pass filter implemented with the MAX40018. Set the operating point based on the power supply voltage and the input signal range. Pay attention that the common mode input range is from -0.1V to V_{DD} - 1.1V. The example circuit sets the operating point at $V_{DD}/2$.

The low cut-off frequency is

$$f_{LOW} = \frac{1}{(2 \times \pi \times R2 \times C2)}$$

The high cut-off frequency is

$$f_{HIGH} = \frac{1}{(2 \times \pi \times R1 \times C1)}$$



Figure 3. Active Band-Pass Filter

Motion Detection Application Circuit

Figure 4 shows a human motion detection circuit using the MAX40018 dual op amp.

The motion sensor is a Murata IRA-S210ST0 pyroelectric passive infrared (PIR) sensor with a typical responsivity (RV) of $4.6mV_{PP}$. With a power supply of 3.3V, the PIR sensor output is biased around 1.0V. Since we are interested in human motion, the frequency range of interest is set to 0.5 Hz to 7 Hz.

The first stage amplifies the PIR sensor output. The high frequency noise is filtered by R3 and C3 feedback filter, with a cutoff frequency $f_{HIGH1} = 1/(2 \times \pi \times R3 \times C3) = 7Hz$. The low frequency noise is filtered by the R1 and C1 high pass filter, with a cutoff frequency $f_{LOW1} = 1/(2 \times \pi \times R1 \times C1) = 0.5$ Hz. The DC signal of the sensor output and the op amp input offset voltage are not amplified, they are showing at the output of the first stage op amp.

The first stage gain is set by G1 = 1 + R3/R1 = 46.3. This gain guarantees the amplified signal will not saturate the first stage op amp, but large enough to distinguish the motion generated signal from the background noise.

The second stage is similar to the first stage. It amplifies the AC component of the signal and rejects the DC component.

The high cutoff frequency $f_{HIGH2} = 1/(2 \times \pi \times R5 \times C5) =$ 7 Hz. The low cutoff frequency is $f_{LOW2} = 1/(2 \times \pi \times R4 \times C4) = 0.5$ Hz. The second stage gain is G2 = 1 + R5/ R4 = 46.3. Similar to the first stage, the input offset voltage does not matter because only AC is amplified. The bias voltage at the noninverting input is set to 1.1V, so that the input has the largest swing between 0V to V_{DD} -1.1V. Use large divider network resistors to reduce power consumption of the system.

The circuit has a GBP requirement of $7Hz \times 46.3 = 324.1Hz$, which is guaranteed by the MAX40018's GBP of 9kHz.

The MAX40018's dual op amps and the ultra-low supply current of 350nA per channel make it a perfect fit for this motion detection circuit.

Dual nanoPower Op Amps in Tiny WLP and TDFN Packages



Figure 4. Motion Detection Circuit



Figure 5. Gas Detection Circuit

Gas Detection Circuit

Figure 5 shows a gas detection circuit using the MAX40018.

The first op amp generates a constant voltage at the sensor reference electrode (RE). The op amp's ultra-low input bias current of 1pA is ideal for this stage. The second op amp converts the sensor output current into a voltage

output. The output voltage V_{OUT} = VREF2 - I_{SENSE} x R3. I_{SENSE} can be positive or negative, depending on the type of the sensor.

The MAX40018's dual op amps, ultra-low current consumption, and ultra-low input bias current minimizes the power requirement of the gas detection circuit, while providing high accuracy and low system cost.

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Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	PACKAGE CODE	TOP MARK
MAX40018ANA+	-40°C to +125°C	WLP-8	N80B1+1	AAK
MAX40018ATA+	-40°C to +125°C	TDFN	T833+2	BAA

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Denotes tape-and-reel.

Dual nanoPower Op Amps in Tiny WLP and TDFN Packages

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/17	Initial release	—
1	4/18	Updated Ordering Information table	12
2	10/19	Updated Pin Configuration and Pin Description	7, 8
3	11/19	Updated Electrical Characteristics table	

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

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