Contact Monitor and Level Shifters with LDO Regulator

General Description

The MAX13037/MAX13038 contact monitor and level shifters monitor and debounce eight remote mechanical switches and assert an interrupt ($\overline{INT}$) if a switch changes state. The state of each switch is sampled through an SPI interface by reading the status register. Any switch can be prohibited from asserting an interrupt by writing to the command register. Four of the switch inputs are intended for ground-connected switches (IN0–IN3) and the other four inputs (IN4–IN7) are programmable in groups of two for either ground-connected or battery-connected switches. Two switch inputs (IN0, IN1) have direct level-shifted outputs (DO0, DO1) to be used for PWM or other timing-based signals.

Switch input thresholds are set to 50% of the voltage applied to BATREF. The threshold hysteresis is set by connecting an external resistor from HYST to ground. The MAX13037/MAX13038 supply an adjustable wetting current to each closed switch to clean mechanical switch contacts that are exposed to adverse conditions.

The MAX13037/MAX13038 feature a low dropout (LDO) linear regulator capable of supplying up to 150mA of current. The MAX13037 LDO has an output voltage of +5V, whereas the MAX13038 has an output voltage of +3.3V. The MAX13037/MAX13038 also feature a watchdog timer and an open-drain reset output with adjustable timing.

The MAX13037/MAX13038 operate with a +6V to +26V battery voltage applied to BAT. The MAX13037/MAX13038 are available in a 6mm x 6mm, 36-pin TQFN package and operate over the automotive -40°C to +125°C temperature range.

Applications

Body Computers

Window Lifters

Seat Movers

Electric Sunroofs

Other Control ECUs

Features

- +6V to +26V Operating Voltage Range
- +42V Compatibility on BAT
- Switch Inputs Withstand Reverse Battery
- 150mA LDO, +5V (MAX13037) or +3.3V (MAX13038)
- Ultra-Low Operating Current 28µA (typ) in 64ms Scan Mode with LDO ON
- Resistor Adjustable Switching Hysteresis
- Watchdog and Reset
- Built-In Switch Debouncing
- Interrupt Output
- Immunity to Transients
- High Modularity
- Thermal Protection
- ±8kV HBM ESD Protection on IN0–IN7 Without External Components
- Two Inputs (IN0, IN1) Programmable as Direct Outputs
- Four Inputs (IN4–IN7) Programmable for BAT or GND Related Switches

Ordering Information

PART	LDO OUTPUT VOLTAGE	TEMP RANGE	PIN-PACKAGE
MAX13037ATX+	+5V	-40°C to +125°C	36 TQFN-EP* (6mm x 6mm)
MAX13038ATX+	+3.3V	-40°C to +125°C	36 TQFN-EP* (6mm x 6mm)

+Denotes a lead(Pb)-free/RoHS-compliant package package.
**EP = Exposed pad.*

Pin Configuration and Typical Application Circuit appear at end of data sheet.

19-1084; Rev 1; 5/15

maxim integrated™

Absolute Maximum Ratings

(All voltages referenced to GND, unless otherwise noted.)

V_{LO} .....-0.3V to +6.0V
BAT.....-0.3V to +42V
IN_ , BATREF.....-45V to +45V
IN_ to BAT .....-45V to +45V
$\overline{SD}$, $\overline{REGON}$.....-0.3V to +45V
HYST, WET, TD, TDEB, THRESH, $\overline{OT}$, $\overline{INT}$, $\overline{RST}$.....-0.3V to 6.0V
$\overline{CS}$, CLK, SDI, SDO, WDI,
DO0, DO1, $\overline{REGOFF}$.....-0.3V to (V_{LO} + 0.3V)

Continuous Current ($\overline{CS}$, CLK, SDI, SDO, WDI, DO0,
DO1, $\overline{REGOFF}$).....±20mA
Continuous Power Dissipation (T_A = +70°C)
36-Pin TQFN (derate 35.7mW/°C above +70°C) 2857mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....28°C/W

Junction-to-Case Thermal Resistance (θ_{JC}) .....1.4°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations see **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(BAT = +6V to +26V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at BAT = +14V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
BAT Supply Range	V_{BAT}			6		26	V
BAT Supply Current with Regulator On	I_{SUP_REG}	V_{BAT} = +14V, continuous scan (SC2 = 1, SC1 = 1, SC0 = 0), programmable hysteresis off (M0 = M1 = 1), IN0–IN7 = unconnected, regulator on ($\overline{REGON}$ = $\overline{REGOFF}$ = GND).			57	110	µA
BAT Supply Current with Regulator Off	I_{SUP}	V_{BAT} = +14V, continuous scan (SC2 = 1, SC1 = 1, SC0 = 0), programmable hysteresis off (M0 = M1 = 1), IN0–IN7 = unconnected, regulator off ($\overline{REGON}$ = BAT, $\overline{REGOFF}$ = GND).			46	80	µA
BAT Supply Current in Scan Mode with Regulator On	I_{SCAN_REG}	V_{BAT} = +14V, scan mode (SC0 = 0, SC1 = 0, SC2 = 0), regulator on ($\overline{REGON}$ = $\overline{REGOFF}$ = GND).			28	48	µA
BAT Supply Current in Scan Mode with Regulator Off	I_{SCAN}	V_{BAT} = +14V, scan mode (SC0 = 0, SC1 = 0, SC2 = 0), regulator off ($\overline{REGON}$ = BAT, $\overline{REGOFF}$ = GND).			17	35	µA
BAT Supply Current in Shutdown Mode	I_{SHDN}	$V_{\overline{SD}}$ = 0V, V_{BAT} = +14V, $\overline{REGON}$ = BAT	T_A = +25°C		3	5	µA
			T_A = +125°C		4	7	
BATREF Input Resistance	R_{BATREF}	V_{BATREF} = +14V		1	2.7		MΩ
BATREF Input Leakage Current in Shutdown	I_{L_BATREF}	$V_{\overline{SD}}$ = 0V, V_{BATREF} = +14V				1	µA

Electrical Characteristics (continued)

(BAT = +6V to +26V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at BAT = +14V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SWITCH INPUTS (IN0–IN7)							
Input Voltage Threshold Center (Note 3)	V_{TH_C}	R_{HYST} = ∞ or programmable hysteresis disabled		0.425 x V_{BATREF}	0.5 x V_{BATREF}	0.575 x V_{BATREF}	V
		R_{HYST} = 90kΩ		0.4 x V_{BATREF}	0.5 x V_{BATREF}	0.63 x V_{BATREF}	
Input Voltage Threshold Hysteresis (Note 4)	V_{TH_HYS}	R_{HYST} = ∞ or programmable hysteresis disabled		0.133 x V_{BATREF}	0.166 x V_{BATREF}	0.22 x V_{BATREF}	V
		R_{HYST} = 90kΩ		0. 26 x V_{BATREF}	0.361 x V_{BATREF}	0. 48 x V_{BATREF}	
		R_{HYST} = 0Ω			0.5 x V_{BATREF}		
Switch-State Sense Resistor	R_{SENSE}			11	16	22	kΩ
Wetting Current Rise/Fall Time (Note 5)	$I_{WET\_RISE\_FALL}$	R_{WET} = 61kΩ	Rise		6		µs
			Fall		1		
Wetting Current	I_{WET}	R_{WET} = 61kΩ			22		mA
		R_{WET} = 30kΩ		28	40	51	
		R_{WET} = 330kΩ			7.5		
IN0–IN7 Input Impedance in Shutdown		$V_{\overline{SD}}$ = 0V, $V_{IN\_}$ = +14V		5.5	8.5		MΩ
ESD Protection IN0–IN7		Human Body Model (HBM)			8		kV
LOGIC-LEVELS ($\overline{CS}$, CLK, SDI , SDI, DO0, DO1, $\overline{INT}$, $\overline{OT}$, $\overline{RST}$, $\overline{SD}$, $\overline{REGON}$, $\overline{REGOFF}$)							
SDO, DO1, DO2 Output Voltage High	V_{OH}	Source current = 2mA		0.8 x V_{LO}			V
SDO, DO1, DO2 Output Voltage Low	V_{OL}	Sink current = 4mA				0.2 x V_{LO}	V
$\overline{INT}$, $\overline{OT}$, $\overline{RST}$ Output Voltage Low	V_{INTL}	Sink current = 4mA				0.4	V
$\overline{SD}$ Input Leakage Current	$I_{L\_\overline{SD}}$	$V_{\overline{SD}}$ = V_{BAT} = +14V				1	µA
$\overline{SD}$, $\overline{REGON}$ Input Voltage Low	$V_{IL\_\overline{SD}}$					0.8	V
$\overline{SD}$, $\overline{REGON}$ Input Voltage High	$V_{IH\_\overline{SD}}$			2.4			V
$\overline{REGON}$ Pullup Current	$I_{\overline{REGON}}$	$\overline{REGON}$ = 0		0.4	1	3.0	µA
$\overline{CS}$, CLK, SDI, $\overline{REGOFF}$, WDI Input Voltage Low	V_{IL}					0.33 x V_{LO}	V
$\overline{CS}$, CLK, SDI, $\overline{REGOFF}$, WDI Input Voltage High	V_{IH}			0.66 x V_{LO}			V
$\overline{CS}$, CLK, WDI, $\overline{REGOFF}$ Input Leakage Current	I_{IL}			-1		+1	µA
$\overline{INT}$, $\overline{OT}$, $\overline{RST}$ Leakage Current	I_{OL}			-1		+1	µA
SDI Pulldown Resistor	R_{SDI}			65	100	145	kΩ

Electrical Characteristics (continued)

(BAT = +6V to +26V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at BAT = +14V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LINEAR REGULATOR							
Output Voltage	V_{LO}	MAX13037, V_{BAT} = +14V, I_{LOAD} = 1mA		4.92	5.00	5.08	V
		MAX13038, V_{BAT} = +14V, I_{LOAD} = 1mA		3.234	3.300	3.366	
Load Regulation	LOAD_REG	I_{LOAD} = 1mA to 50mA, V_{BAT} = +14V	V_{LO} = +5V (MAX13037)		0.53	1	%
			V_{LO} = +3.3V (MAX13038)		0.53	1	
		I_{LOAD} = 1mA to 150mA, V_{BAT} = +14V	V_{LO} = +5V (MAX13037)		1	1.85	
			V_{LO} = +3.3V (MAX13038)		1	1.85	
Line Regulation	LINE_REG	V_{BAT} = +6V to +26V		-0.9		+0.9	mV/V
Dropout Voltage	V_{DROP}	V_{LO} = +5V, I_{LO} = 50mA (MAX13037)				330	mV
		V_{LO} = +5V, I_{LO} = 150mA (MAX13037)				1000	
		V_{LO} = +3.3V, I_{LO} = 150mA (MAX13038)				1300	
Output Current Limit	I_{LIM}	V_{BAT} = +14V		150			mA
Power-Supply Rejection Ratio	PSRR	I_{LO} = 10mA, f = 100Hz, 500mV_{P-P}, AC-coupled into V_{BAT}			68		dB
Start-Up Time	t_{START}				1		ms
RESET, WATCHDOG							
Reset Reference Voltage	V_{RST}	THRESH from high to low		1.20	1.24	1.28	V
THERMAL SHUTDOWN							
Thermal Shutdown Temperature	T_{SHDN}	(Note 6)			165		°C
Thermal Shutdown Temperature for Wetting Currents Only	T_{WARN}	(Note 7)			135		°C
Thermal Shutdown Hysteresis	T_{HYST}				15		°C

Timing Characteristics

(BAT = +6V to +26V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at BAT = +14V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN0 to DO0 Propagation Delay, IN1 to DO1 Propagation Delay	t_{PROP}	V_{BAT} = +6V		22	35	µs
		V_{BAT} = +14V		22		
CLK Frequency	f_{CLK}	Input rise/fall time < 2ns			5	MHz
Falling Edge of $\overline{CS}$ to Rising Edge of CLK Required Setup Time	t_{LEAD}	Input rise/fall time < 2ns, Figure 1	110			ns
Falling Edge of CLK to Rising Edge of $\overline{CS}$ Required Setup Time	t_{LAG}	Input rise/fall time < 2ns, Figure 1	50			ns

Timing Characteristics (continued)

(BAT = +6V to +26V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at BAT = +14V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDI to Falling Edge of CLK Required Setup Time	$t_{SI(SU)}$	Input rise/fall time < 2ns, Figure 1	30			ns
Falling Edge of CLK to SDI Required Hold Time	$t_{SI(HOLD)}$	Input rise/fall time < 2ns, Figure 1	20			ns
Time from Falling Edge of $\overline{CS}$ to SDO Low Impedance	$t_{SO(EN)}$	Input rise/fall time < 2ns, Figure 1			55	ns
Time from Rising Edge of $\overline{CS}$ to SDO High Impedance	$t_{SO(DIS)}$	Figures 1 and 2			55	ns
Time from Rising Edge of CLK to SDO Data Valid	t_{VALID}	C_{SDO} =15pF, Figure 1			70	ms
Debounce Time	t_{DEB}	C_{TDEB} = 500pF	3.18	5.9	9.42	ms
		C_{TDEB} = 10nF	63	120	188	ms
Scanning Time Pulse	t_{SCAN}		130	250	400	µs
Scanning Time Period	t_{SCAN-P}	SC0 = 0, SC1 = 1, SC2 = 1	4	8	14	ms
Wetting Time Pulse	t_{WETT}	WTOFF = 0	10	21	35	ms
Time from Shutdown to Normal Operation	t_{SD}	$\overline{SD}$ low-to-high transition to input monitoring enabled		200		µs
Time from SCAN Mode to Normal Operation	t_{SM}	(Note 8)		500		µs
Reset Output Pulse Width	t_{RST}	C_{TD} = 10nF (Figure 3)	10	21	36	ms
Watchdog Timeout Period 1	t_{WD1}	C_{TD} = 10nF, time before $\overline{INT}$ goes low (Figure 3)	40	84	144	ms
Watchdog Timeout Period 2	t_{WD2}	C_{TD} = 10nF, time before $\overline{RST}$ goes low (Figure 3)		2 x t_{WD1}		ms
Minimum Watchdog Timeout Reset on WDI	t_{WDI}		300			ns

Note 2: All units are 100% production tested at T_A = 125°C. Limits over the operating temperature range are guaranteed by design and not production tested.
Note 3: $V_{TH\_C} = (V_{TH\_HIGH} + V_{TH\_LOW}) / 2$.
Note 4: $V_{TH\_HYS} = (V_{TH\_HIGH} - V_{TH\_LOW})$.
Note 5: Wetting current rise/fall time is measured as the time it takes to go from 20% to 80% of the maximum wetting current.
Note 6: T_{SHDN} is the temperature at which the wetting currents and LDO are disabled.
Note 7: T_{WARN} is the temperature at which only the wetting currents are disabled.
Note 8: When exiting SCAN mode to enter Normal Mode (through SPI) any input change is ignored for 500µs (typ) to allow correct wake-up of input comparators. After this time elapses, the inputs are monitored in continuous mode.

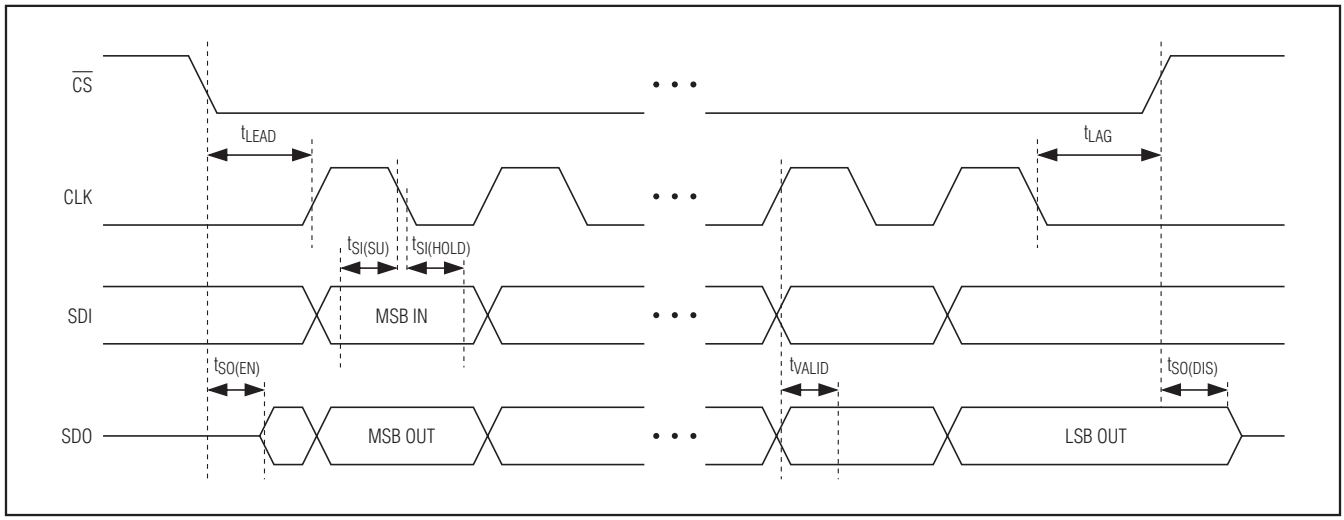


Figure 1. SPI Timing Characteristics

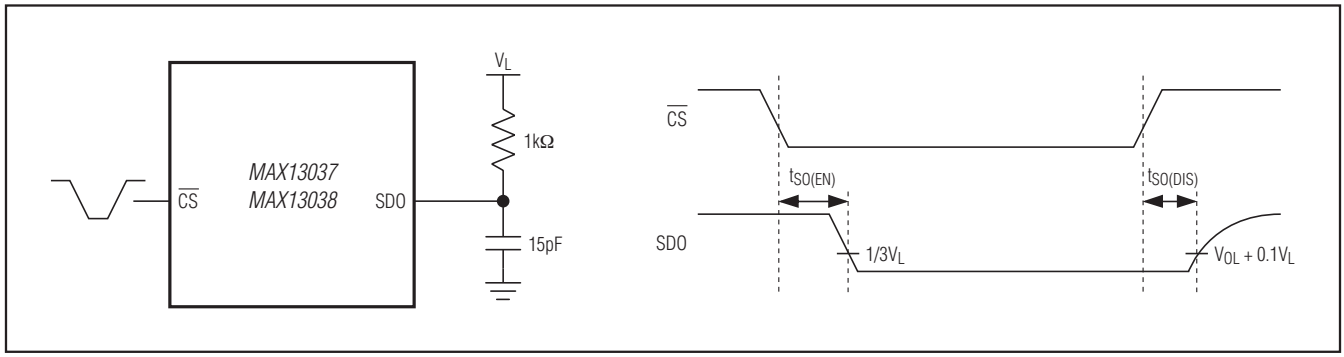


Figure 2. SDO Enable/Disable Test Circuit and Timing Diagram

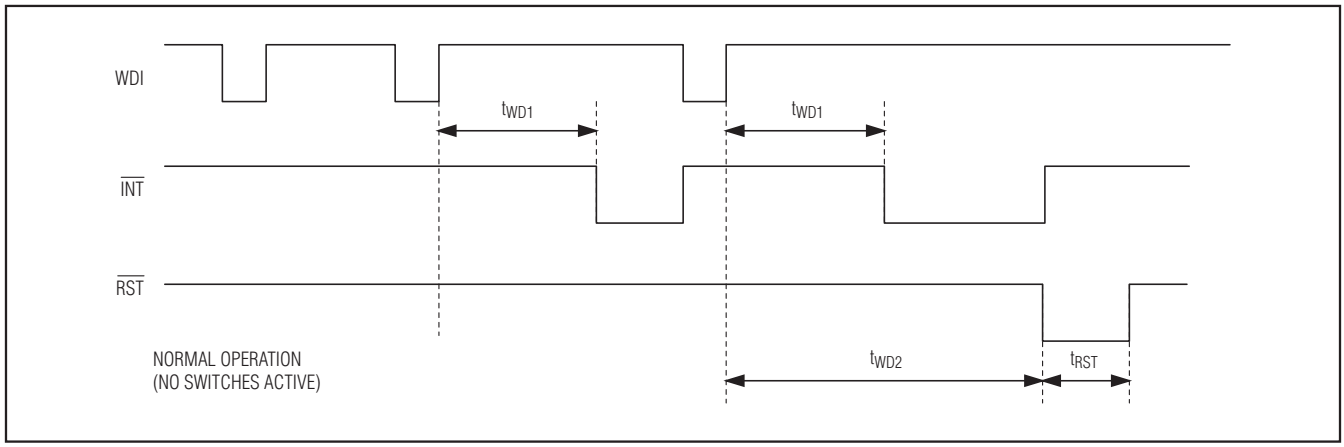
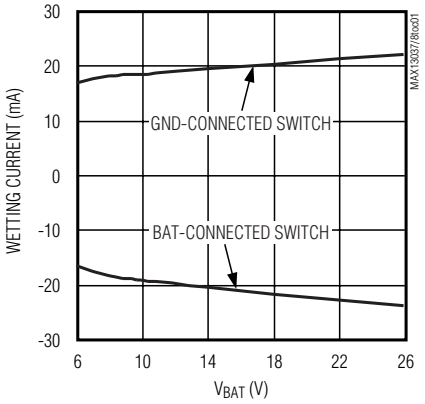


Figure 3. Watchdog Interrupt/Reset Timing Diagram

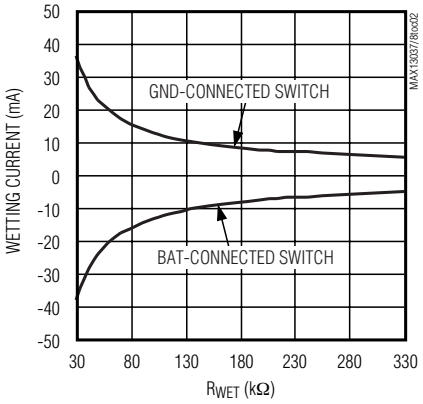
Typical Operating Characteristics

(BAT = +14V, $\overline{SD}$ = V_{BAT}, R_{WET} = 61kΩ, R_{HYST} = 90kΩ, C_{TDEB} = 4700pF, C_{TD} = 4700pF, T_A = +25°C, unless otherwise noted.)

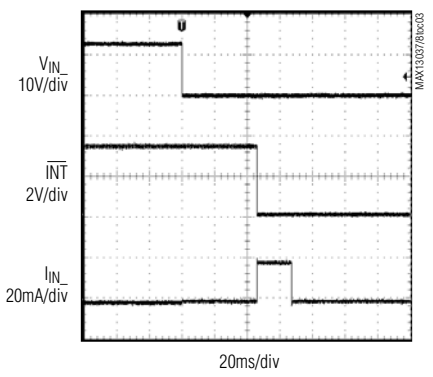
WETTING CURRENT vs. V_{BAT}



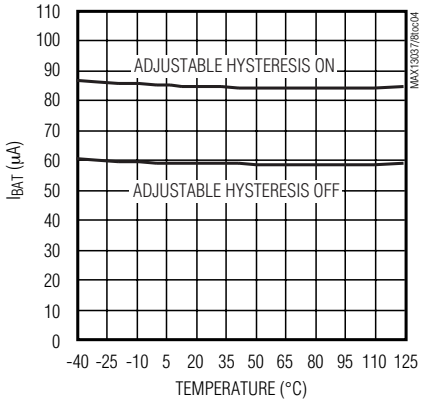
WETTING CURRENT vs. R_{WET}



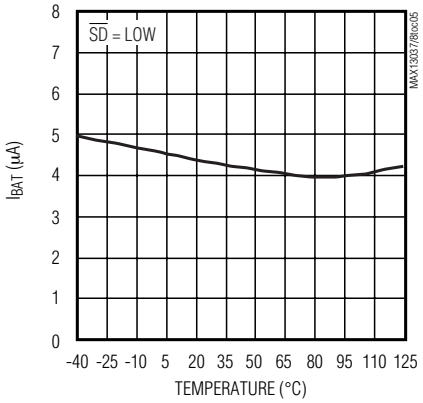
WETTING CURRENT PULSE (NORMAL MODE, WTOFF = 0, WEN = WEND = 1)



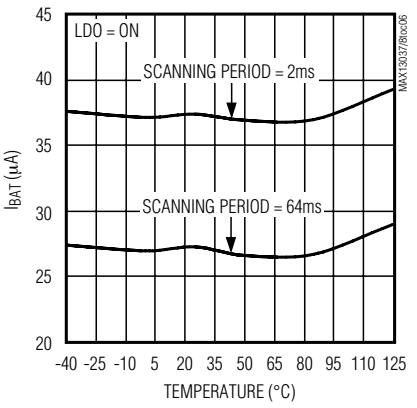
BAT CURRENT vs. TEMPERATURE (NORMAL MODE)



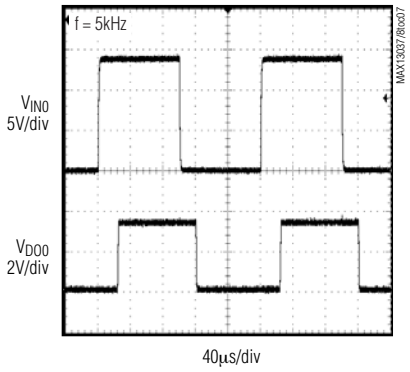
BAT CURRENT vs. TEMPERATURE (NORMAL MODE)



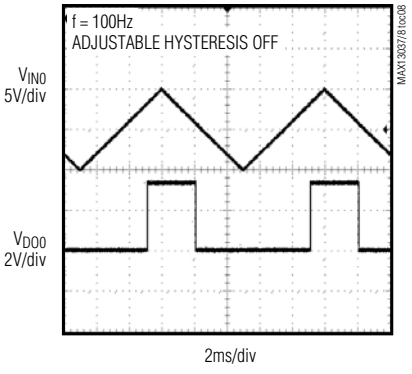
BAT CURRENT vs. TEMPERATURE (SCANNING MODE)



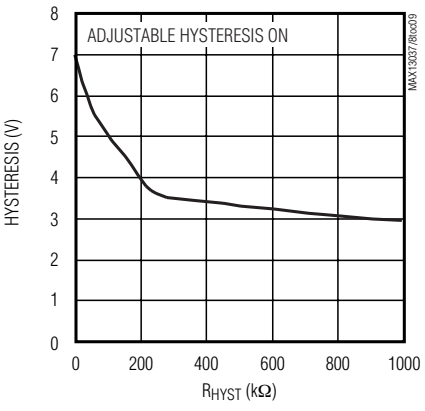
TYPICAL INO DRIVING (NORMAL MODE, WTOFF = WEN = WEND = 0)



TYPICAL INO DRIVING (NORMAL MODE, WTOFF = WEN = WEND = 0)



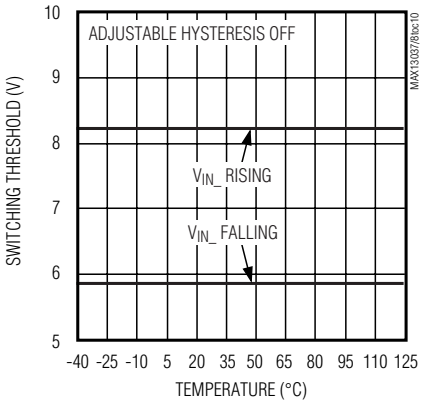
HYSTERESIS vs. R_{HYST}



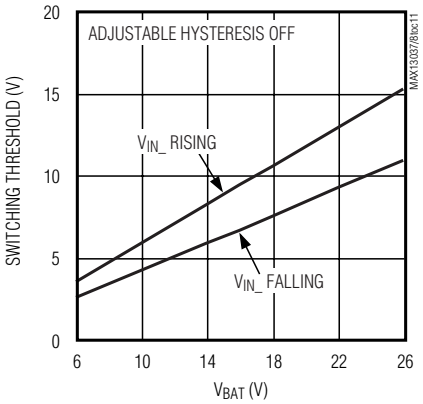
Typical Operating Characteristics (continued)

(BAT = +14V, $\overline{SD}$ = V_{BAT}, R_{WET} = 61kΩ, R_{HYST} = 90kΩ, C_{TDEB} = 4700pF, C_{TD} = 4700pF, T_A = +25°C, unless otherwise noted.)

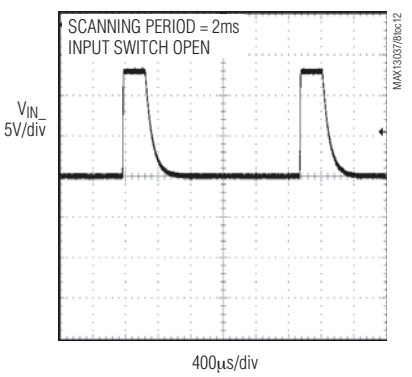
SWITCHING THRESHOLD vs. TEMPERATURE



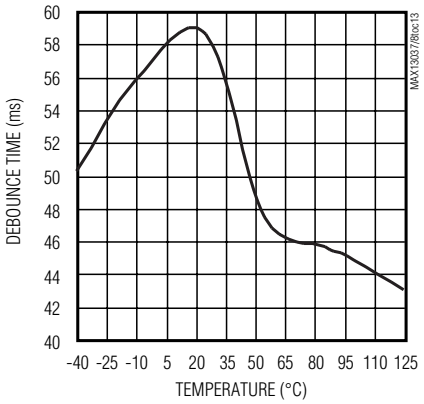
SWITCHING THRESHOLD vs. V_{BAT}



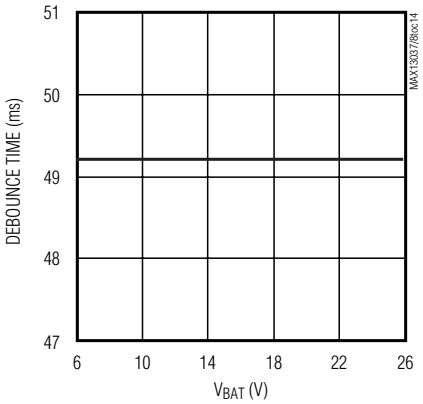
INPUT WAVEFORM IN SCAN MODE (SCAN MODE, WTOFF = WEN = 0, WEND = 1)



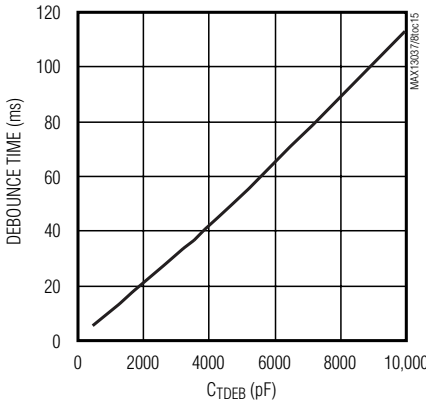
DEBOUNCE TIME vs. TEMPERATURE



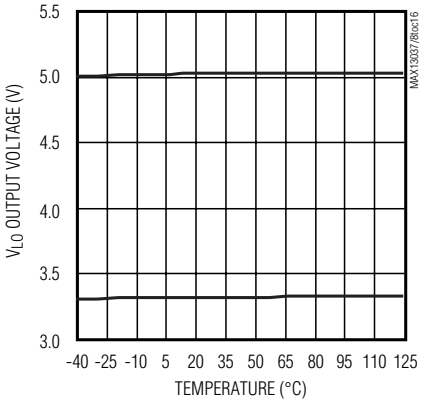
DEBOUNCE TIME vs. BAT VOLTAGE



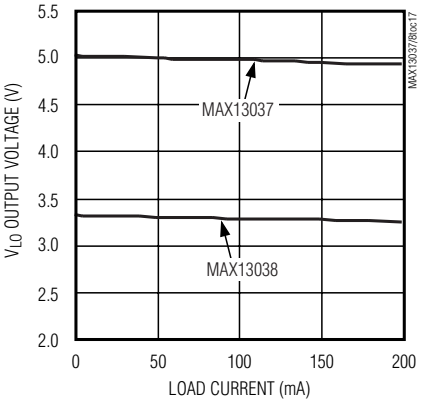
DEBOUNCE TIME vs. C_{TDEB}



V_{LO} OUTPUT VOLTAGE vs. TEMPERATURE



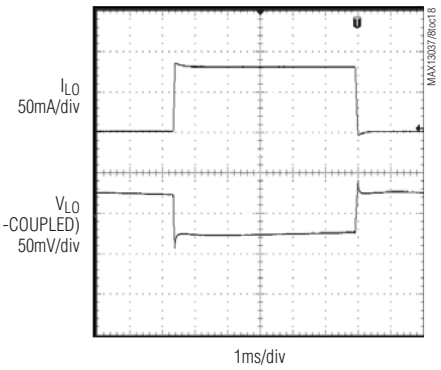
V_{LO} OUTPUT VOLTAGE vs. LOAD CURRENT



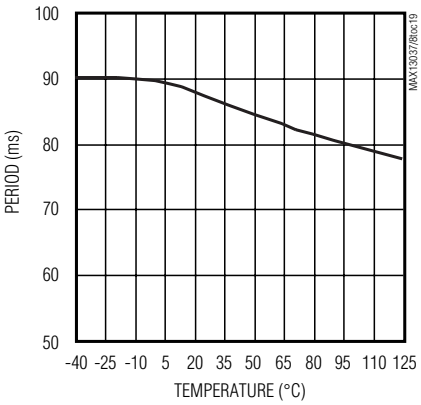
Typical Operating Characteristics (continued)

(BAT = +14V, $\overline{SD}$ = V_{BAT}, R_{WET} = 61kΩ, R_{HYST} = 90kΩ, C_{TDEB} = 4700pF, C_{TD} = 4700pF, T_A = +25°C, unless otherwise noted.)

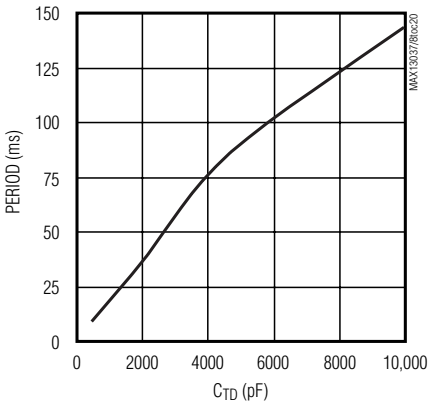
V_{LO} TRANSIENT LOAD REGULATION



WATCHDOG INTERRUPT AND RESET PERIOD vs. TEMPERATURE



WATCHDOG INTERRUPT AND RESET PERIOD vs. C_{TD}



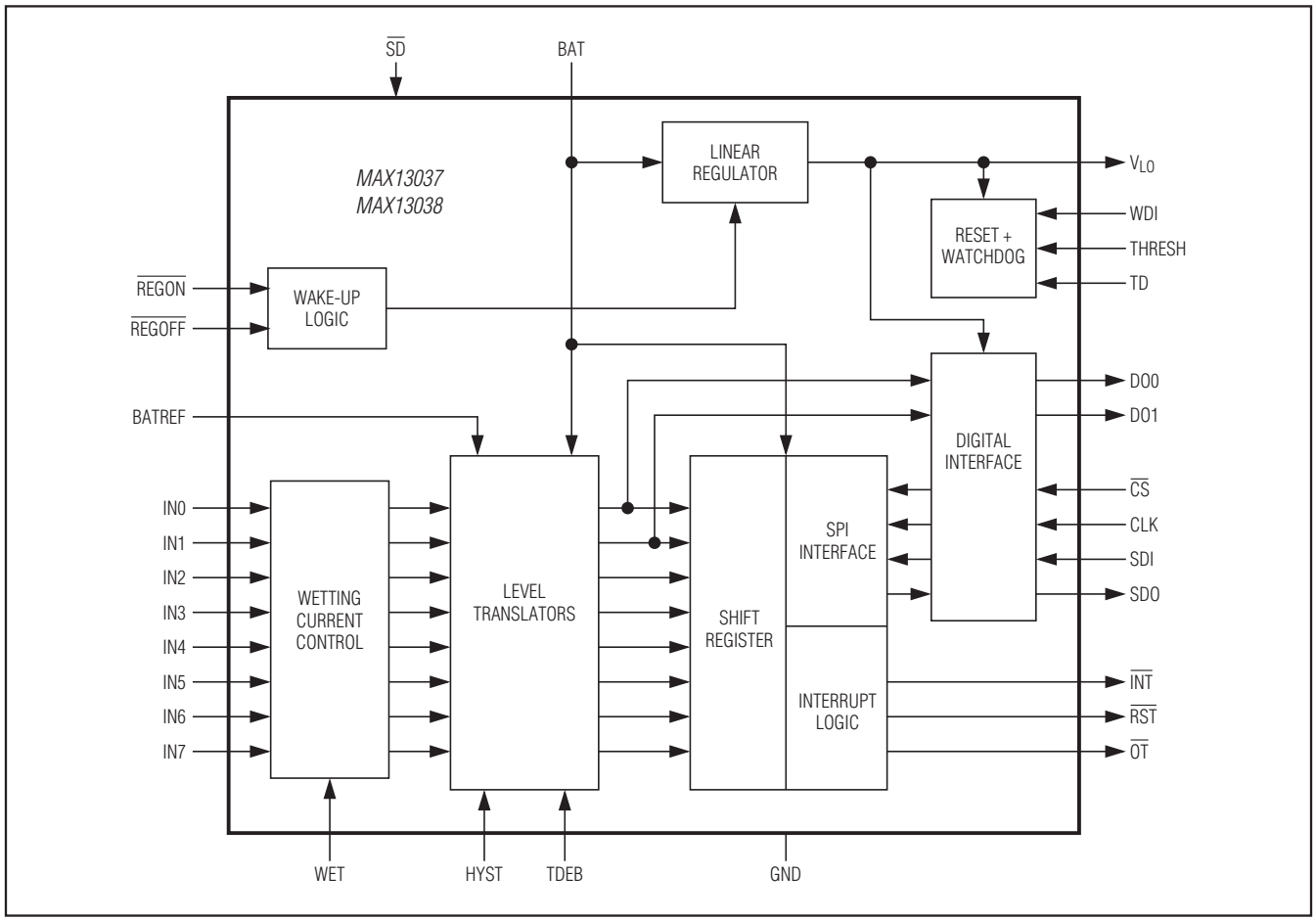
Pin Description

PIN	NAME	FUNCTION
1, 15, 31	GND	Ground
2	IN0	Switch Input Channel 0. Connect IN0 to a switch connected to GND. IN0 can be programmed as a direct input with a level-shifted output on DO0 (see the *Mechanical Switch Inputs (IN0–IN7)* section).
3	IN1	Switch Input Channel 1. Connect IN1 to a switch connected to GND. IN1 can be programmed as a direct input with a level-shifted output on DO1 (see the *Mechanical Switch Inputs (IN0–IN7)* section).
4	IN2	Switch Input Channel 2. Connect IN2 to a switch connected to GND.
5	IN3	Switch Input Channel 3. Connect IN3 to a switch connected to GND.
6	IN4	Switch Input Channel 4. Connect IN4 to a switch connected to GND or BAT.
7	IN5	Switch Input Channel 5. Connect IN5 to a switch connected to GND or BAT.
8	IN6	Switch Input Channel 6. Connect IN6 to a switch connected to GND or BAT.
9	IN7	Switch Input Channel 7. Connect IN7 to a switch connected to GND or BAT.
10, 11, 34	N.C.	No Connection. Not internally connected.
12	HYST	Hysteresis Input. Connect HYST to GND with a 0Ω to 900kΩ resistor to set the input voltage hysteresis on IN0–IN7.
13	WET	Wetting Current Input. Connect a 30kΩ to 330kΩ resistor from WET to GND to set the wetting current on IN0–IN7.
14	TDEB	Switch Debounce Time Input. Connect a 500pF to 10nF capacitor from TDEB to GND to set the switch debounce time.
16	$\overline{OT}$	Overtemperature Warning Output. $\overline{OT}$ is an open-drain output that asserts low when the thermal warning threshold is exceeded.
17	$\overline{INT}$	Interrupt Output. $\overline{INT}$ is an open-drain output that asserts low when one or more of the IN0–IN7 inputs change state and are enabled for interrupts or when the watchdog times out.
18	TD	Reset and Watchdog Timeout Input. Connect TD to GND with a 500pF to 10nF capacitor to set the timeout period for the reset and watchdog.

Pin Description (continued)

PIN	NAME	FUNCTION
19	$\overline{SD}$	Shutdown Input. Drive $\overline{SD}$ low to place the MAX13037/MAX13038 into shutdown mode and disable the linear regulator. Drive $\overline{SD}$ high for normal operation. $\overline{SD}$ is compatible with voltages up to V_{BAT}.
20	$\overline{REGON}$	Linear Regulator Enable Input (Active Low). Connect $\overline{REGON}$ to $\overline{INT}$ to enable a wake-up when a switch status change is detected. Drive $\overline{REGON}$ using an open-drain logic output to control the regulator directly. $\overline{REGON}$ is internally pulled up to an internal bias voltage of approximately +4.8V.
21	$\overline{REGOFF}$	Linear Regulator Disable Input (Active Low). $\overline{REGOFF}$ is used in conjunction with $\overline{REGON}$ when the internal regulator is enabled by an interrupt (see the *Low-Dropout Linear Regulator (V_{LO})* section).
22	$\overline{CS}$	SPI Chip-Select Input. Drive $\overline{CS}$ low to enable the clocking of data into and out of the MAX13037/MAX13038. SPI data is latched into the MAX13037/MAX13038 on the rising edge of $\overline{CS}$.
23	SDO	SPI Serial-Data Output. SPI data is output on SDO on the rising edges of CLK while $\overline{CS}$ is held low. SDO is three-state when $\overline{CS}$ is high.
24	SDI	SPI Serial-Data Input. SPI data is latched into the internal shift register on the falling edges of CLK while $\overline{CS}$ is held low. SDI has an internal 100kΩ pulldown resistor.
25	CLK	SPI Serial-Clock Input
26	$\overline{RST}$	Reset Output. $\overline{RST}$ is an open-drain output that asserts low when V_{LO} is below the threshold determined by the THRESH input. $\overline{RST}$ also asserts low when the watchdog times out.
27	DO1	Data Output Channel 1. DO1 is the level-shifted output of IN1 when WEND = 0.
28	DO0	Data Output Channel 0. DO0 is the level-shifted output of IN0 when WEND = 0.
29	THRESH	Reset Threshold Level Input. Connect THRESH to a resistor divider between V_{LO} and GND to set the reset reference level.
30	WDI	Watchdog Timer Input. The watchdog timer is reset at every transition on the WDI input.
32	BATREF	Battery Reference Input. Switch thresholds are set to 50% of the voltage applied to BATREF. Connect BATREF to the system's battery supply voltage.
33	V_{LO}	Linear Regulator Output. V_{LO} is the output of an internal linear regulator and is the reference voltage for all digital I/O. Bypass V_{LO} with a 2.2µF or greater ceramic capacitor. Alternatively, a 10µF electrolytic capacitor can be used in parallel with a 0.1µF ceramic capacitor.
35, 36	BAT	Battery Supply Input. Connect BAT to a positive +6V to +26V battery supply voltage. Bypass BAT to ground with a 0.1µF ceramic capacitor and a 10µF electrolytic capacitor placed as close as possible to BAT.
—	EP	Exposed Paddle. Connect EP to GND.

Functional Diagram



Detailed Description

The MAX13037/MAX13038 contact monitor and level shifters monitor and debounce eight remote mechanical switches and assert an interrupt ($\overline{INT}$) if a switch changes state. Any of the switch inputs can be prohibited from asserting an interrupt. The switch threshold levels are set to 50% of the voltage applied to BATREF and all switch inputs feature a common adjustable hysteresis, debounce time, and wetting current. Two switch inputs (IN0, IN1) are programmable to have direct outputs (DO0, DO1), useable for PWM or other timing-based signals.

The MAX13037/MAX13038 feature an SPI interface to monitor individual switch inputs and to configure interrupt masking, hysteresis, and wetting current enable/disable, switch configuration (battery-connected or ground-connected), and scanning period.

The MAX13037/MAX13038 provide an internal low dropout (LDO) linear regulator capable of supplying up to 150mA. The LDO can be enabled or disabled through two digital control inputs: $\overline{REGON}$ and $\overline{REGOFF}$. A watchdog timer and power-on reset circuitry is provided on the MAX13037/MAX13038 to supervise external microcontrollers (µC).

The MAX13037/MAX13038 feature three modes of operation: normal mode, scanning mode, and shutdown mode. In normal mode, the part is fully functional and internal sensing resistors are connected to all switch inputs. In scanning mode, the sensing resistors are connected for a finite duration to reduce power consumption. In shutdown mode, all switch inputs are high impedance and the internal LDO is switched off to further reduce power consumption.

BAT

BAT is the main power-supply input. Bypass BAT to ground with a 0.1µF ceramic capacitor placed as close as possible to BAT. In addition, bypass BAT with a 10µF or greater capacitor. BAT can withstand DC voltages up to +42V.

Low-Dropout Linear Regulator (V_{LO})

The MAX13037/MAX13038 contain an internal LDO linear regulator supplied by the BAT input. The LDO output voltage is present on V_{LO} and is capable of supplying up to 150mA of current. The MAX13037 output voltage is set to +5V and the MAX13038 output voltage is set to +3.3V.

The LDO regulator is controlled through the $\overline{REGON}$ and $\overline{REGOFF}$ inputs as shown in Figure 4. $\overline{REGON}$ is an input able to withstand voltages up to V_{BAT}. The LDO startup time is 1ms (typ).

There are two options for controlling the linear regulator:

- **Wake-Up on Interrupt:** In this case, $\overline{REGON}$ is connected to $\overline{INT}$ and when the MAX13037/MAX13038 generate an interrupt, the linear regulator is turned on, thus providing power to the local µCs. The µC pulls $\overline{REGOFF}$ high to keep the regulator on before making an SPI read (which causes $\overline{INT}$ and $\overline{REGON}$ to go high). The linear regulator can then be turned off by pulling $\overline{REGOFF}$ low.
- **Direct Control:** In this case, the regulator is enabled/disabled by some other signal in the system which must be connected to $\overline{REGON}$. If $\overline{REGOFF}$ is not used, it must be connected to GND to allow the turnoff of the LDO.

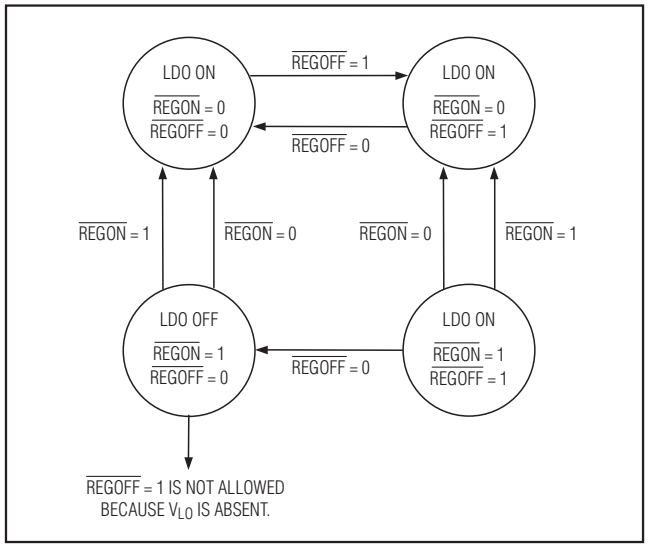


Figure 4. Linear Regulator State Diagram

Linear Regulator Wake-Up

Regulator wake-up can be controlled with the $\overline{INT}$ output by connecting it to $\overline{REGON}$. $\overline{REGON}$ is a TTL input with an internal pullup to a low-voltage internal reference of +4.8V (typ). With this control scheme, any change of the input switches (enabled for interrupt generation) causes the regulator to turn on, thus providing power to any external circuitry connected to V_{LO}. If an external microcontroller is supplied from V_{LO}, the microcontroller can keep the LDO on by forcing $\overline{REGOFF}$ high. Reading from the MAX13037/MAX13038 over the SPI interface causes the $\overline{INT}$ output to go into high-impedance so that both $\overline{INT}$ and $\overline{REGON}$ are pulled high. After this phase, the microcontroller can turn off the regulator again by driving $\overline{REGOFF}$ low.

Note that it is also possible to tie multiple open-drain active-low outputs in an ORing configuration, allowing the wakeup of the regulator from other devices.

If the $\overline{INT}$ output is not used to control the regulator, connect the $\overline{REGOFF}$ input to ground and use $\overline{REGON}$ to enable or disable the regulator as shown in Figure 4.

Watchdog Timer (WDI)

The MAX13037/MAX13038 feature a watchdog timer that is reset on every transition on the WDI input. If there is no transition on WDI before the first timeout period (t_{WD1}) the $\overline{INT}$ output asserts low. If there is still no transition on WDI after the second timeout period (t_{WD2}), the $\overline{RST}$ output is pulsed low for t_{RST} and the $\overline{INT}$ output deasserts (see Figure 3). The watchdog timeout period can be adjusted by changing the capacitor value on the TD input.

$$t_{RST}\ (ms) = 2 \times C_{TD}\ (nF)$$

$$t_{WD1} = 4 \times t_{RST}\ (ms)$$

$$t_{WD2} = 8 \times t_{RST}\ (ms)$$

Note that WDI can be tied to the $\overline{CS}$ input to allow a watchdog reset for every read/write operation over the SPI interface. To avoid any corruption of the internal command register, it is necessary to transmit the full programming word (16 bits) for every $\overline{CS}$ negative pulse.

Reset Output ($\overline{RST}$)

The $\overline{RST}$ output asserts low when a watchdog timeout occurs or when the LDO output voltage drops below a certain threshold. The threshold voltage is set by connecting an external voltage divider on the THRESH input between V_{LO} and GND. The voltage on THRESH is compared with an internal reference voltage of +1.24V and if it is lower, the $\overline{RST}$ output asserts low for t_{RST} and remains low if V_{LO} does not rise above the threshold.

Mechanical Switch Inputs (IN0–IN7)

IN0–IN7 are the inputs for remote mechanical switches. The status of each switch input is indicated by the SW0 through SW7 bits in the status register, and each switch input can be programmed to not assert an interrupt ($\overline{INT}$) by writing to the P0–P7 bits in the command register. All switch inputs are configured to assert an interrupt upon power-up.

The first four inputs (IN0–IN3) are intended for ground-connected switches. The remaining four inputs (IN4–IN7) can be programmed in sets of two for either ground-connected or battery-connected switches by writing to the M0 and M1 bits (see Table 5). The default state after power-up is IN2–IN7 configured for ground-connected switches, and IN0/IN1 configured for direct inputs.

All switch inputs have internal 16kΩ sense resistors to detect switch transitions. Inputs configured for ground-connected switches are pulled up to BAT and inputs configured for battery-connected switches are pulled down to GND. Figure 5 shows the switch input structure for IN0 and IN1. IN0 and IN1 can be programmed as direct inputs with level-shifted outputs (DO0 and DO1) by clearing the WEND bit in the command register (normal mode only). When programmed as direct inputs, IN0 and IN1 can be used for PWM or other signaling. Clearing the WEND bit disables the sense resistors and wetting currents on IN0 and IN1. When programmed as direct inputs, the status of IN0 and IN1 is not reflected in the status register, and interrupts are not allowed on these inputs.

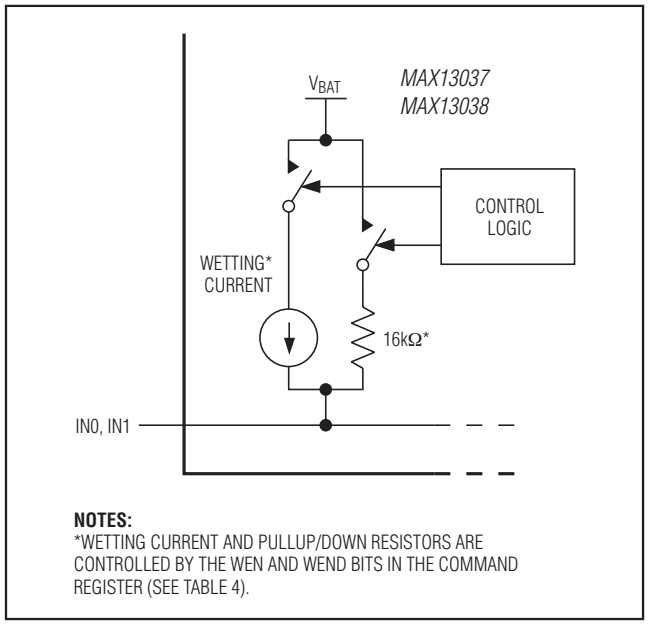


Figure 5. Input Structure of IN0 and IN1

Switch Threshold Levels and Hysteresis (BATREF, HYST)

Input thresholds for the remote switches are 50% of the voltage applied to BATREF. The BATREF input is typically connected to the battery voltage before the reverse-battery protection diode. The MAX13037/MAX13038 feature adjustable hysteresis on the switch inputs by connecting an external 0 to 900kΩ resistor from HYST to ground (normal mode only). Short HYST to ground to obtain the maximum hysteresis of (0.5 x V_{BATREF}). The approximate formula for hysteresis is given below:

$$V_{HYST} = \left[0.166 + \frac{43}{(123 + (R_{HYST(k\Omega)})}\right](V_{BATREF})$$

To reduce power consumption, the adjustable hysteresis can be disabled by setting [SC2:SC1:SC0 = 1:1:0] in the command register. When the adjustable hysteresis is disabled, the hysteresis is set to 0.166 x V_{BATREF}.

Switch Debounce and Deglitch

The switch inputs IN0–IN7 share a common programmable debounce timer to increase the noise immunity of the system in normal and scan mode. The switch debounce time is set by connecting a capacitor between the t_{DEB} input and ground. The minimum value of this capacitor is 500pF and the maximum value is 10nF, corresponding to a debounce time of 5ms to 100ms respectively. To calculate other debounce times the following formula should be used:

$$C(nF) = t_{DEB}(ms) / 10$$

All switch input glitches of less than 20µs in duration are automatically rejected by the MAX13037/MAX13038.

Debounce in Normal Mode

When a change of state occurs at the switch input the debounce timer starts. If the new state is stable for at least t_{DEB}, the status register is updated and an interrupt is generated (if enabled). If the input returns to its previous state before the debounce time has elapsed, an interrupt is not generated and the status register is not updated.

Debounce in Scan Mode

A change of state at the switch input causes the device to automatically enter normal mode and the debounce timing to start. The device remains in normal mode as long as the input state differs from the previous state. As soon as the debounce time ends, the status register is updated, an interrupt is generated, and the device re-enters scan mode.

If the input returns to its previous state before the end of the debounce time, the device re-enters scan mode, an interrupt is not generated, and the status register is not updated.

Wetting Current (WET)

The MAX13037/MAX13038 feature adjustable wetting current to any closed switch to clean switch contacts that are exposed to adverse conditions. The wetting current is set by connecting a 30kΩ to 330kΩ resistor from WET to ground. A 30kΩ resistor corresponds to a wetting current of 40mA (typ) and a 330kΩ resistor corresponds to a 4mA (typ) wetting current. See the *Typical Operating Characteristics* section for the relationship between the wetting current and R_{WET}.

The WEN and WEND bits in the command register enable and disable the wetting currents and the WTOFF bit allows the wetting current to be activated for a duration of 20ms (typ) (see the *Command Register* section). Disabling wetting currents, or limiting the active wetting current time reduces power consumption. The default state upon power-up is all wetting currents disabled.

Wetting current is activated on closed switches just after the debounce time. The wetting current pulse starts after the debounce time. A wetting current pulse is provided to all closed switches when a valid input change is detected. Wetting current rise and fall times are controlled to enhance EMC performance. There is one wetting current timer for all switch inputs. Therefore, it is possible to observe wetting pulses longer than expected whenever two switches turn on in sequence and are spaced out less than t_{WET}. In scan mode, the wetting current is enabled during the polling pulse only.

When using wetting currents, special care must be taken to avoid exceeding the maximum power dissipation of the MAX13037/MAX13038 (see the *Applications Information* section).

Switch Outputs (DO0, DO1)

DO0 and DO1 are direct level-shifted outputs of the switch inputs IN0 and IN1 when the WEND bit of the command register is cleared and when operating in normal mode. When configured as direct inputs, the wetting currents and sensing resistors are disabled on IN0 and IN1. DO0 and DO1 are three-stated when the WEND bit is set or when operating in scan mode.

When programmed as direct inputs, the status of IN0 and IN1 are not reflected in the status register and interrupts are not allowed on these inputs.

Interrupt Output ($\overline{INT}$)

$\overline{INT}$ is an active-low, open-drain output that asserts when any of the switch inputs change state, as long as the particular input is enabled for interrupts (set by clearing P7–P0 in the command register). $\overline{INT}$ also asserts when the first watchdog timeout period elapses (t_{WD1}). A pullup resistor to V_{LO} is needed on $\overline{INT}$. $\overline{INT}$ is cleared when $\overline{CS}$ is driven low for a read/write operation.

The $\overline{INT}$ output still asserts when V_{LO} is disabled provided that it is pulled up to a different supply voltage.

Thermal Protection ($\overline{OT}$)

The MAX13037/MAX13038 feature a two-level thermal protection strategy that prevents the device from being damaged by overheating. At the initial warning temperature of +135°C (typ), only wetting currents are disabled. The MAX13037/MAX13038 return to normal operation after the internal temperature decreases below +120°C (typ). This protection feature is disabled when WEN = 0 or when all inputs are open. At the second thermal warning temperature of +170°C (typ), the LDO is shut down. Because a µC is often supplied by the LDO, an overheating event caused by excessive power dissipation related to I/O wetting currents is normally resolved without affecting the µC status.

An open-drain, active-low output ($\overline{OT}$) asserts low when the internal temperature of the device rises above the thermal warning threshold. $\overline{OT}$ is immediately cleared when the $\overline{CS}$ input is driven low for read/write operations, regardless of whether the temperature is above the threshold, or not. The overtemperature status of the MAX13037/MAX13038 can also be monitored by reading the OT bit in the status register. The OT bit is set when the internal temperature rises above the temperature threshold, and it is cleared when the temperature falls below the temperature hysteresis level. This allows a µC to monitor the overtemperature status, even if the $\overline{OT}$ output has been cleared. See Figure 6 for an example timing diagram of the overtemperature alerts.

If desired, the $\overline{OT}$ and $\overline{INT}$ outputs can be connected to the same µC GPIO in a wired-OR configuration to save a µC pin. The $\overline{OT}$ output still asserts when V_L is absent provided that it is pulled up to a different supply voltage.

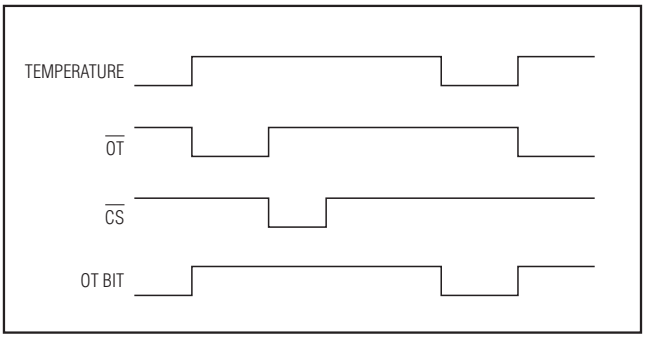


Figure 6. Example Timing Diagram of the Overtemperature Alerts

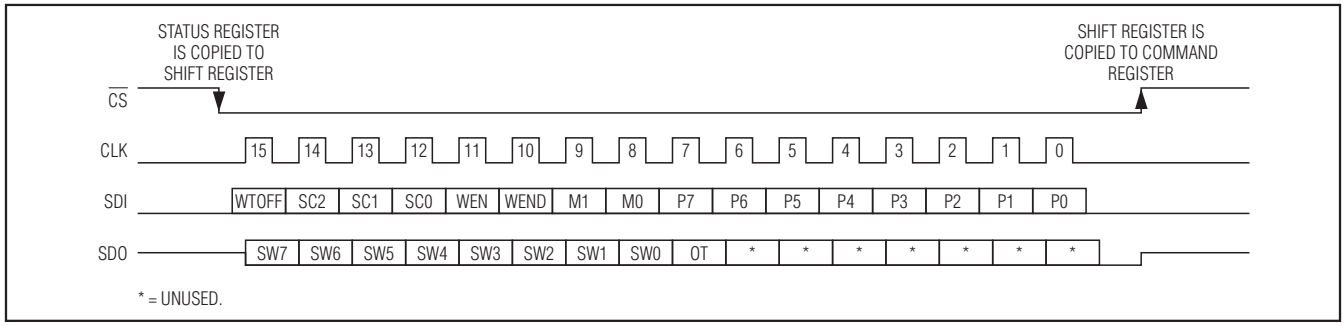


Figure 7. SPI Read/Write Example

Serial Peripheral Interface (CS, SD0, SDI, CLK)

The MAX13037/MAX13038 operate as a Serial Peripheral Interface (SPI) slave devices. An SPI master accesses the MAX13037/MAX13038 by reading from a status register and writing to a command register. Both registers are 16 bits long and are accessed most significant bit (MSB) first.

On the falling edge of $\overline{CS}$, the status register is immediately loaded to an internal shift register and the contents are transferred out of the SDO output on the rising edge of CLK. Serial data on the SDI input is latched into the shift register on the falling edge of CLK. On the rising edge of $\overline{CS}$, the contents of the shift register are copied to the command register (see Figure 7). The status and command registers are 16 bits wide, so it is essential to clock a total of 16 bits while $\overline{CS}$ is low for the input and output data to be valid. When $\overline{CS}$ is high, the SDO output is high-impedance and any transitions on CLK and SDI are ignored. The $\overline{INT}$ and $\overline{OT}$ flags are cleared on the $\overline{CS}$ falling edge. Input status changes occurring during the $\overline{CS}$ reading/writing operation are allowed. If a switch status changes when $\overline{CS}$ is low, the interrupt is asserted as usual. This allows the part to be used even if V_{LO} is disabled provided that the $\overline{INT}$ output is pulled up to another supply voltage.

Status Register

The status register contains the status of the switches connected to IN7 through IN0 and it also contains an overtemperature warning bit (see Table 1). The status register is accessed through an SPI-compatible master.

Notes:

Bits 15–8: Switch 7 Through 0 Status (SW7–SW0)

SW7 through SW0 reflect the status of the switches connected to inputs IN7 through IN0, respectively. Open switches are returned as a [0] and closed switches are returned as a [1].

Bit 7: Overtemperature Warning (OT)

The OT bit returns a [1] when the internal temperature of the MAX13037/MAX13038 is above the temperature warning threshold of +135°C (typ). The OT bit returns a [0] when the MAX13037/MAX13038 is either below the temperature threshold, or it has fallen below the temperature hysteresis level following an overtemperature event.

Bits 6–0: Unused

Bits 6 through 0 are unused and should be ignored.

Command Register

The command register is used to configure the MAX13037/MAX13038 for various modes of operation and is accessed by an SPI-compatible master (see Table 2). The power-on reset (POR) value of the command register is 0x00.

Table 1. Status Register

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0	OT	—	—	—	—	—	—	—

Table 2. Command Register

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	WTOFF	SC2	SC1	SC0	WEN	WEND	M1	M0	P7	P6	P5	P4	P3	P2	P1	P0
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Notes:

Bit 15: Wetting Current Mode (WTOFF)

Set the WTOFF bit to configure the wetting currents as continuous on closed switches. Clear the WTOFF bit to configure the wetting current as a pulse where the wetting current is turned on for a set duration of 20ms after a switch closes (and the debounce is timed out). After 20ms elapses, the wetting current is turned off. Either wetting current mode is only applicable to switches that have wetting currents enabled (see WEN and WEND bits). In scan mode, the wetting currents are on for the polling time of 250µs (typ) and are pulsed at the programmed scanning period. When WTOFF is set, the wetting current continuously pulses at the programmed scanning period. When WTOFF is cleared, the wetting current pulses at the programmed scanning period, but turns off after 20ms elapses.

Bits 14, 13, 12: Scanning Period (SC2, SC1, SC0)

The SC2, SC1, and SC0 bits are used to program the scanning period as depicted in Table 3. Switch inputs are simultaneously polled for a finite duration of 250µs (typ), and polling occurs at a period selected through the SC2, SC1, and SC0 inputs. Figure 8 shows a timing diagram of switch scanning and sampling. When the inputs are not being polled, the sense resistors are disconnected, reducing the current consumption caused from polling closed switches. For a continuous scanning period ([SC2:SC1:SC0] = [1:1:1] or [1:1:0]), the switch inputs are constantly being monitored and the sense resistors are always connected. The state [SC2:SC1:SC0] = [1:1:0] also disables adjustable hysteresis (normally set by R_{HYST}) and fixes hysteresis at 0.166 x V_{BATREF}. When adjustable hysteresis is not needed, it is recommended to disable this feature to reduce power consumption.

Bit 11: Global Wetting Current Enable (WEN)

The WEN bit is a global enable for the wetting currents on all the channels. Set the WEN bit to enable wetting currents on all channels and clear the WEN bit to disable wetting currents. Even with wetting currents globally enabled, the wetting currents and sense resistors on IN0 and IN1 can still be turned off with the WEND bit (see Table 4).

Bit 10: IN0 and IN1 Wetting Current Enable (WEND)

The WEND bit is used to turn on wetting currents and sense resistors on inputs IN0 and IN1. Set the WEND bit to enable wetting currents on IN0 and IN1 and clear the WEND bit to turn off the wetting current and sense resistors on IN0 and IN1. When the wetting currents and sense resistors are disabled (WEND = 0), IN0 and IN1 are configured as direct inputs with level-shifted outputs on DO0 and D01. DO0 and DO1 can only be used as level-shifted outputs in normal mode and are three-stated in scan mode (see the *Scan Mode* section). Note that both the WEN and WEND bits need to be set for wetting currents to be enabled on IN0 and

Table 3. Programmable Scanning Period

SC2	SC1	SC0	SCANNING PERIOD (ms)
0	0	0	64
0	0	1	32
0	1	0	16
0	1	1	8
1	0	0	4
1	0	1	2
1	1	0	Continuous/adjustable hysteresis off
1	1	1	Continuous

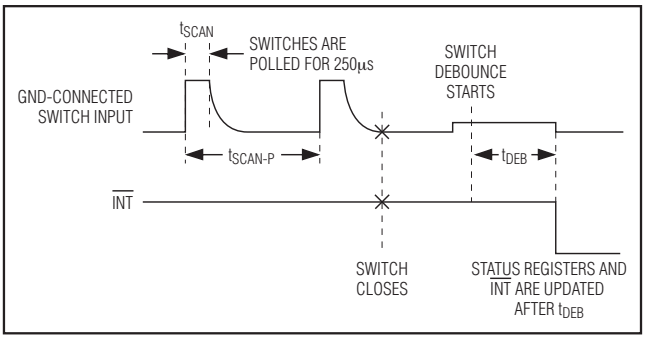


Figure 8. Switch Sampling in Scan Mode

Table 4. Truth Table for WEN and WEND

WEN	WEND	WETTING CURRENT (IN0, IN1)	16kΩ SENSE RESISTOR (IN0, IN1)	WETTING CURRENT (IN2–IN7)	16kΩ SENSE RESISTOR (IN2–IN7)
0	0	Off	Off	Off	On
0	1	Off	On	Off	On
1	0	Off	Off	On	On
1	1	On	On	On	On

Table 5. Switch Configuration Controlled by M1 and M0

M1	M0	IN7 AND IN6 SWITCH CONFIGURATION	IN5 AND IN4 SWITCH CONFIGURATION	IN3–IN0 SWITCH CONFIGURATION
0	0	Ground	Ground	Ground
0	1	Ground	Battery	Ground
1	0	Battery	Ground	Ground
1	1	Battery	Battery	Ground

IN1 (see Table 4). The DO0 and DO1 outputs are three-stated when WEND = 1. When programmed as direct inputs (WEND = 0), any input changes on IN0 and IN1 are not reflected by the status register.

Bits 9 and 8: Switch Configuration for IN7–IN4 (M1, M0)

The M1 and M0 bits set the switch configuration in groups of two for IN7 through IN4 (see Table 5). Set M1 to configure IN7 and IN6 for battery-connected switches and clear M1 for ground-connected switches. Set M0 to configure IN5 and IN4 for battery-connected switches and clear M0 for ground-connected switches.

Bits 7–0: Interrupt Enable for IN7–IN0 (P7–P0)

The P7 through P0 bits allow independent control of whether inputs IN7 through IN0 generate an interrupt ($\overline{INT}$). Set any bit to disable interrupts on the corresponding input and clear the bit to enable interrupts on the corresponding channel. An interrupt is asserted when any input configured for interrupts changes state. IN0 and IN1 do not generate an interrupt when configured as direct inputs (WEND = 0).

Operating Modes

The MAX13037/MAX13038 feature three modes of operation: normal mode, scan mode, and shutdown mode. Normal mode is entered when the scanning period bits in the command register are configured for continuous scanning ([SC2:SC1:SC0] = [1:1:1] or [1:1:0]). Scan mode is entered when the scanning period bits are set for a periodic scanning time as shown in Table 3. Shutdown mode is entered by driving the shutdown input ($\overline{SD}$) low. The default mode after power-up is scan mode (when $\overline{SD}$ = high) with a scan period of 64ms.

Normal Mode (Continuous Scanning)

In normal mode, the input sense resistors are always connected to the switch inputs to detect any input status change (except IN0 and IN1 when WEND = [0]). Wetting currents are enabled according to the WEN, WEND, and WTOFF bits in the command register. If adjustable hysteresis is not required, this feature can be disabled to reduce power consumption (see the *Typical Operating Characteristics*) by setting the scanning period bits in the command register to ([SC2:SC1:SC0] = [1:1:0]). The hysteresis is set to 0.166 x V_{BATREF} when adjustable hysteresis is disabled.

Scan Mode

In scan mode, each sense resistor is connected for a finite duration of 250µs (typ) and is repeated at a period according to the scanning period bits SC2, SC1, and SC0 (see Table 3). All input resistors are connected simultaneously and the inputs are polled at the same time. When all external switches are open and the scanning period is set to 64ms the scanning mode reduces current consumption to typically 28µA (LDO on) and 17µA (LDO off). Wetting currents (if enabled) are applied to closed switches during the polling time of 250µs (typ) and are pulsed at the programmed scanning period. When WTOFF is set, the wetting current continuously pulses at the programmed scanning period. When WTOFF is cleared, the wetting current pulses at the programmed scanning period, but turns off after 20ms elapses. Inputs IN0 and IN1 cannot be used as direct inputs (WEND = 0) in scan mode. When configured as direct inputs in scan mode, the outputs DO0 and DO1 are high impedance. The quiescent current for a given scan mode can be calculated by the following formula (LDO off):

$$I_{BAT(\mu A)} = 16 \times \left(1 + \frac{1}{t_{SCAN\_P(ms)}}\right)$$

Where V_{BAT} = $\overline{SD}$ = +14V, I_{BAT} is the BAT current expressed in microamps and t_{SCAN_P} is the scanning period expressed in milliseconds.

Shutdown Mode

In shutdown mode, the LDO is disabled, all switch inputs are high impedance and the external switches are no longer monitored, reducing current consumption on BAT to 2.85µA (typ). The MAX13037/MAX13038 reset upon entering shutdown mode and the contents of the command register are lost. Exit shutdown mode by bringing the voltage on $\overline{SD}$ above +2.4V. The $\overline{SD}$ input is compatible with voltages up to V_{BAT}. The MAX13037/MAX13038 take 200µs (typ) to exit shutdown

at which point the command register is restored to its power-up default (0x00) and the MAX13037/MAX13038 enter scan mode. Note that $\overline{SD}$ is compatible with both logic and BAT voltage levels. Having $\overline{SD}$ compatible to V_{BAT} allows the MAX13037/MAX13038 to retain the settings in the command register as well as input monitoring even when V_{LO} is disabled, provided that $\overline{SD}$ = V_{BAT}.

Applications Information

Considerations for Reverse-Battery Tolerance

The BATREF and IN0–IN7 inputs can withstand voltages down to -45V without damage so that reverse battery is not an issue. The BAT input should be protected with a reverse-battery diode as shown in the *Typical Application Circuit*. The shutdown ($\overline{SD}$) and $\overline{REGON}$ inputs can be controlled from a battery-level source, but should be protected against reverse battery in the application.

Power Dissipation

Wetting currents and the LDO output current can result in overheating the MAX13037/MAX13038. At the early thermal warning threshold of +135°C (typ), wetting currents are disabled. This allows the LDO output to remain enabled if overheating is caused by the wetting currents. At temperatures above +170°C, the LDO is also turned off to avoid damage to the device.

It is important to consider the effects of wetting currents on the power dissipated by the MAX13037/MAX13038. For example, assume all inputs are configured for a continuous wetting current of 25mA, all external switches have an on-resistance of 1Ω and the battery voltage is +16V. If all switches are simultaneously closed, the corresponding power dissipated due to wetting currents only is (16V - (25mA x 1Ω)) x 25mA x 8 = 3.12W, which is higher than the absolute maximum power dissipation of 2857mW at +70°C.

The LDO is a second source of power dissipation. For example, if V_{LO} = +3.3V, I_{LO} = 100mA and V_{BAT} = +16V, the power dissipated by the LDO is (16V - 3.3V) + (0.1) = 1.27W. Both the LDO and wetting currents should be taken into account for correct use of the MAX13037/MAX13038.

ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The IN7–IN0 inputs have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±8kV without damage.

Human Body Model

The MAX13037/MAX13038 IN7–IN0 pins are characterized for ±8kV ESD protection using the Human Body Model. Figure 7a shows the Human Body Model, and Figure 7b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

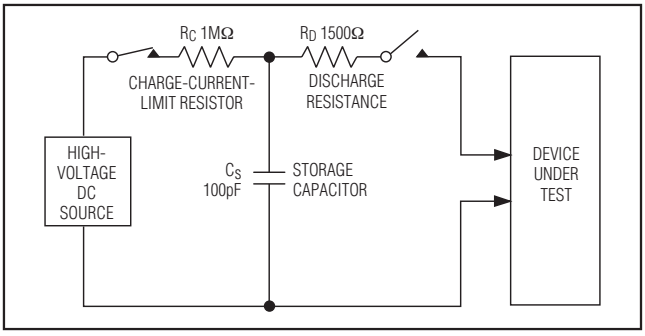


Figure 7a. Human Body ESD Test Model

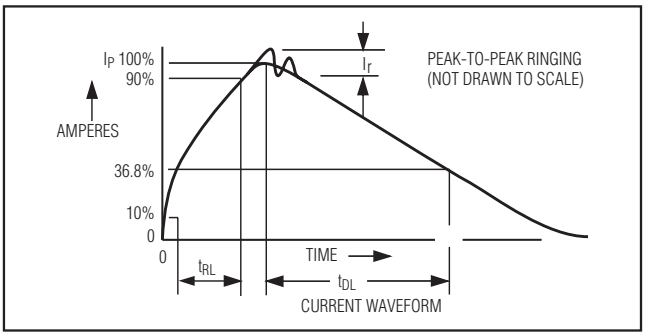
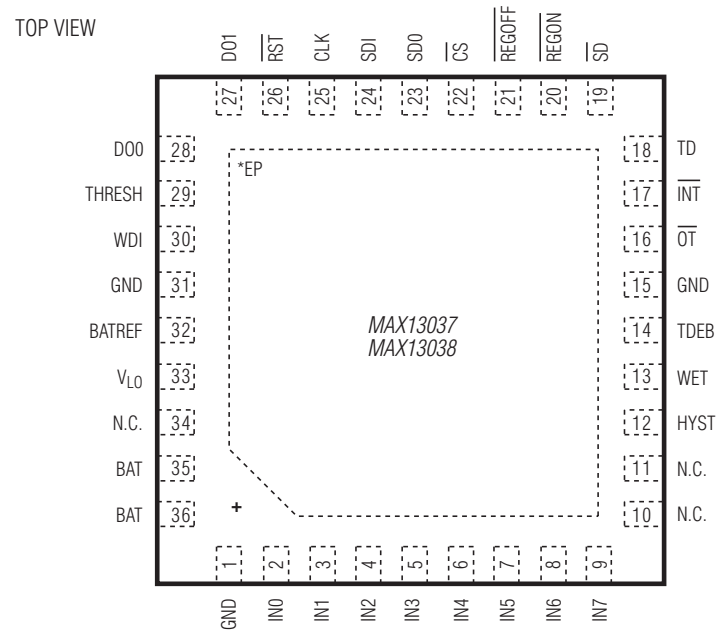


Figure 7b. Human Body Model Current Waveform

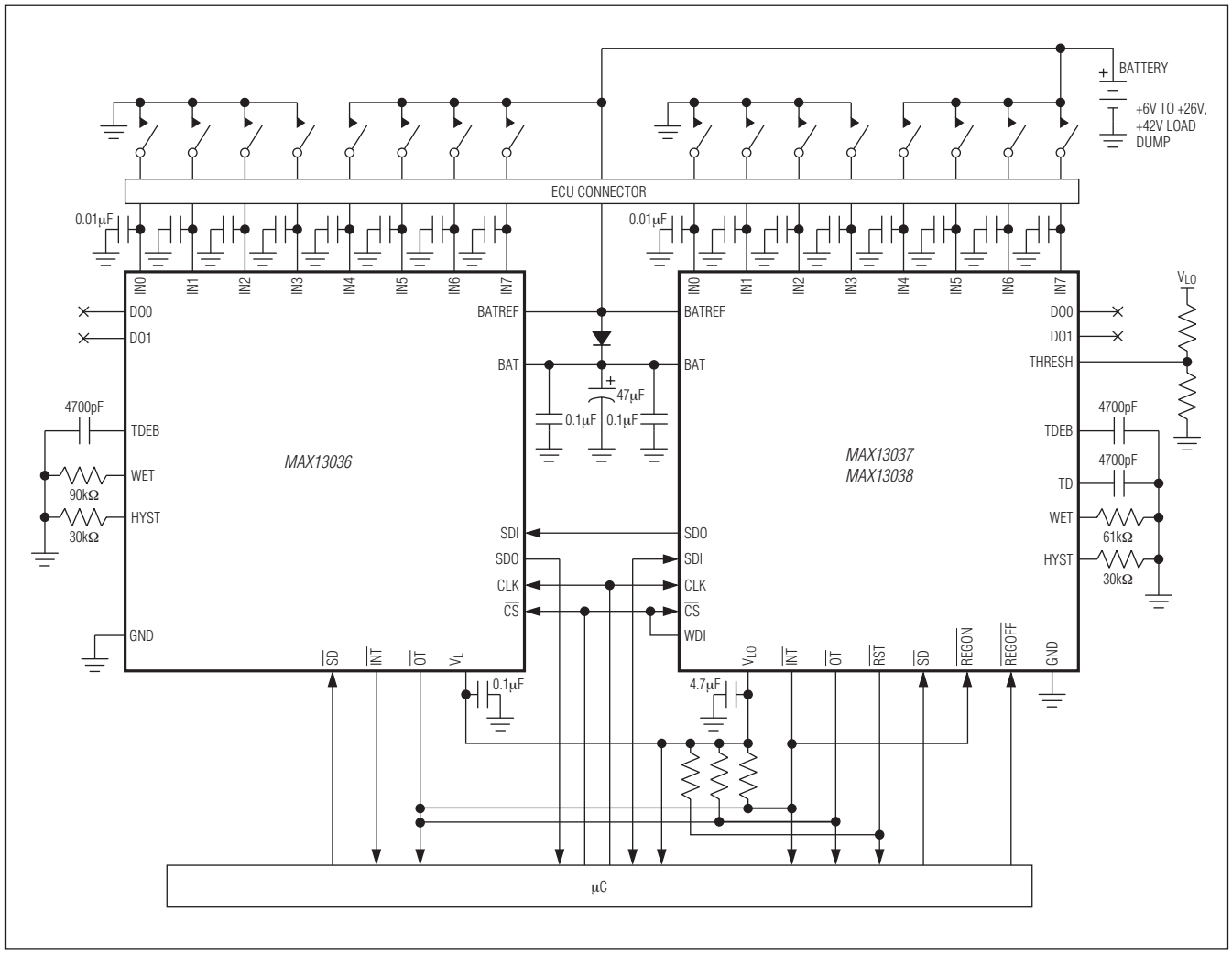
Pin Configuration



TQFN
(6mm x 6mm)

*CONNECT EXPOSED PAD TO GROUND

Typical Operating Circuit



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
36 TQFN-EP	T3666+3	21-0141	90-0050

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/07	Initial release	—
1	5/15	No /V OPNs; deleted automotive references in *General Description* and *Applications Information* sections; added *Package Thermal Characteristics*, updated *Package Information*, and added *Revision History;* rebranded to new Maxim logo	1, 2, 18, 21, 22

