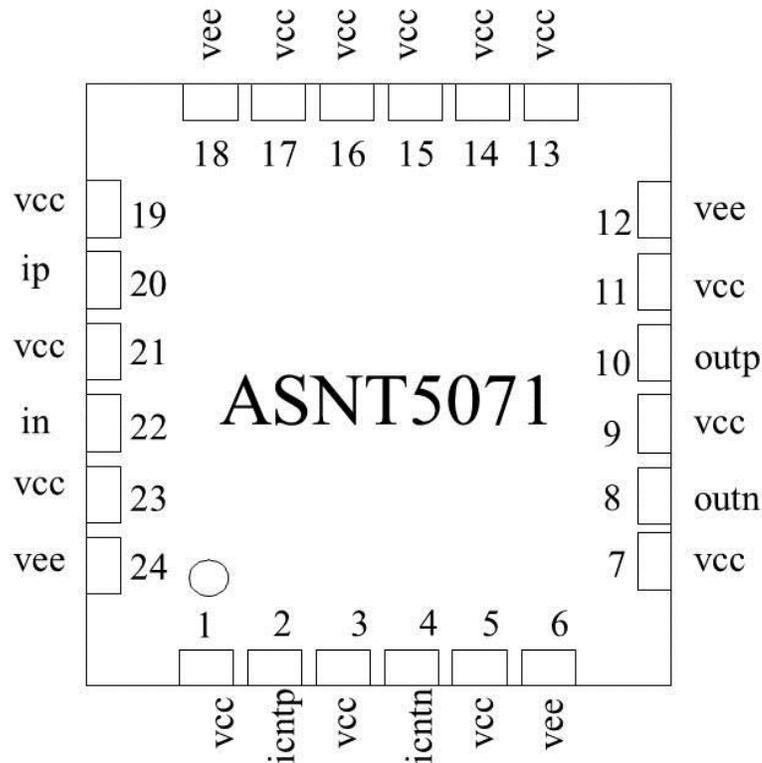




## ASNT5071-PQC DC-17Gbps/10GHz Phase Shifter

- Broadband (DC-17Gbps/DC-10GHz) tunable data/clock phase shifter
- Delay adjustment range of 320ps
- Exhibits low jitter and limited temperature variation over industrial temperature range
- 100MHz of bandwidth for the phase adjustment tuning ports
- Fully differential CML input interfaces
- Fully differential CML output interface with 600mV single-ended swing
- Single +3.3V or -3.3V power supply
- Power consumption: 1.44W
- Fabricated in SiGe for high performance, yield, and reliability
- Standard MLF/QFN 24-pin package



## DESCRIPTION

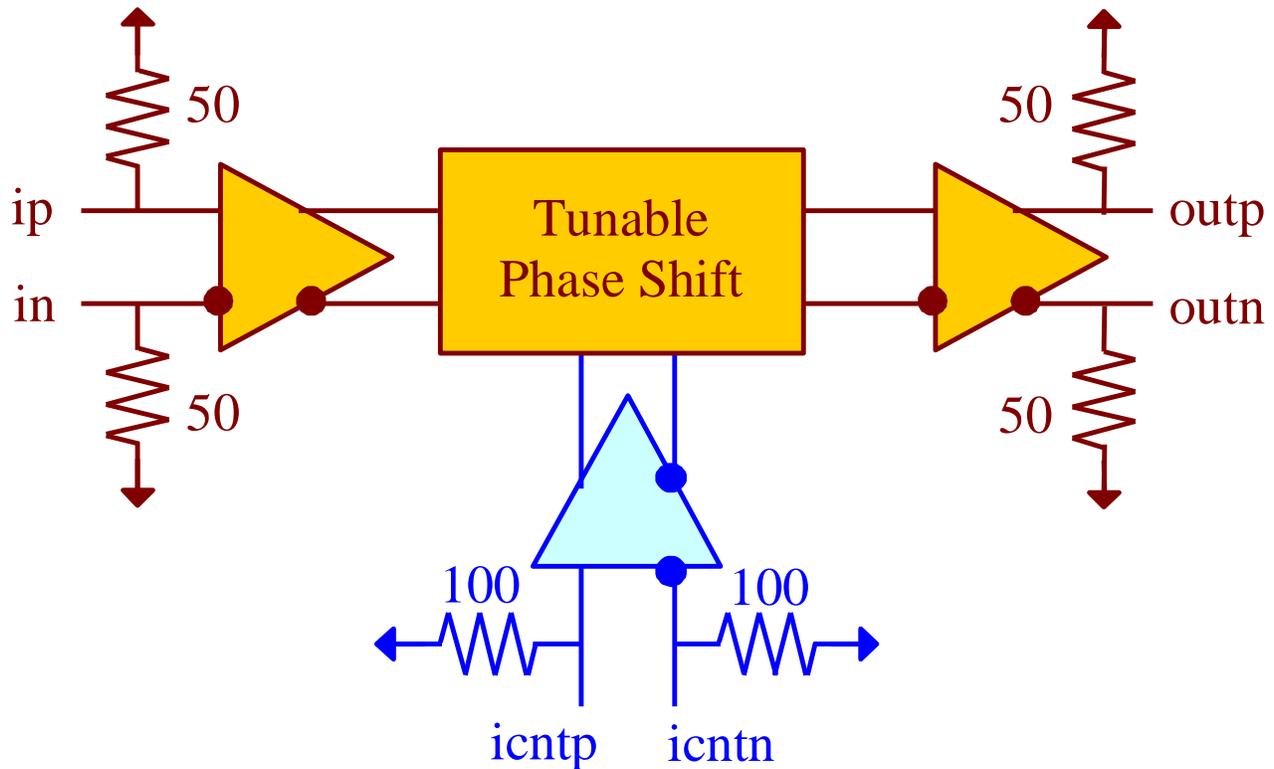


Fig. 1. Functional Block Diagram

ASNT5071-PQC is a data / clock variable delay line fabricated in SiGe technology. The IC shown in Fig. 1 provides an adjustable delay of its differential output signal **outp/outn** in relation to its broadband input signal **ip/in**. The delay adjustment range is temperature-stabilized. The delay is controlled through a wide-band differential tuning port **icntp/icntn**.

The part's I/O's support the CML logic interface with on chip  $50\Omega$  termination to **vcc** and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

Due to an extremely low jitter, the part is suitable for use in high-speed measurement / test equipment.

### Delay Control Port

The delay is controlled through a wide-band differential tuning port **icntp/icntn**. The simulated delay control diagram is shown in Fig. 2.

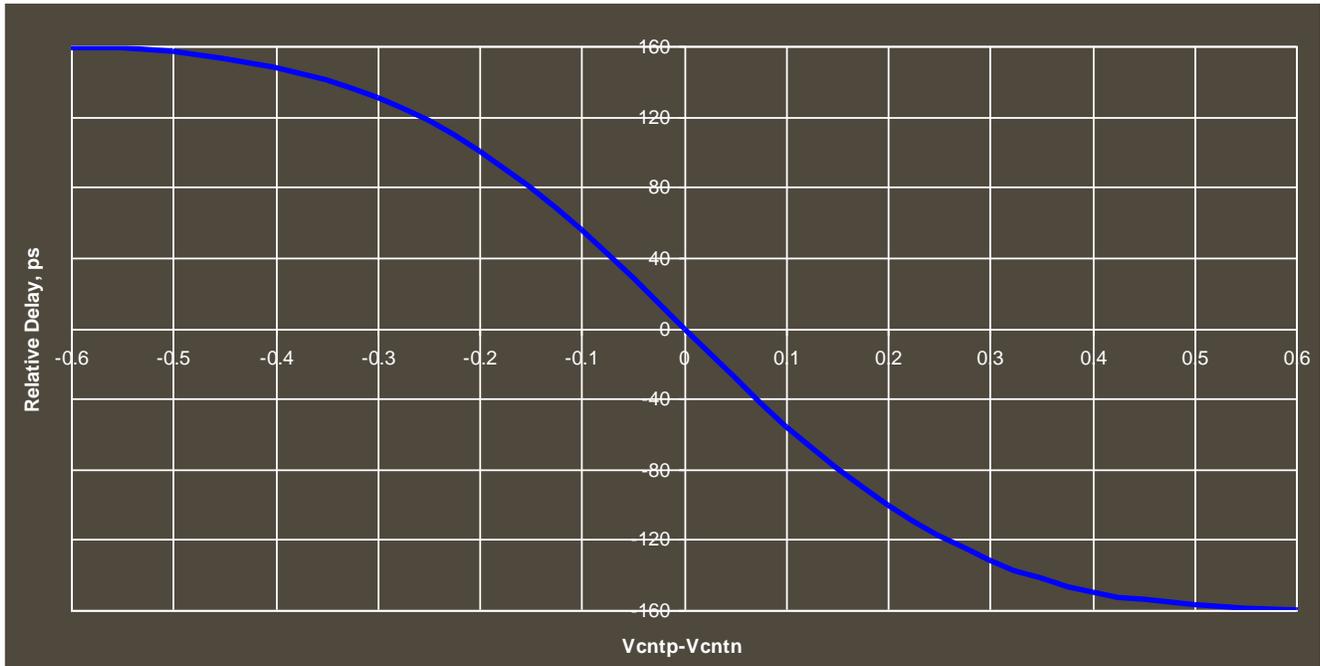


Fig. 2. Delay Control Diagram



## POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply ( $v_{cc} = 0.0V = \text{ground}$  and  $v_{ee} = -3.3V$ ), or a positive supply ( $v_{cc} = +3.3V$  and  $v_{ee} = 0.0V = \text{ground}$ ). In case of a positive supply, all I/Os need AC termination when connected to any devices with  $50\Omega$  termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume  $v_{cc} = 0.0V$  and  $v_{ee} = -3.3V$ .

## ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage ( $v_{ee}$ )		-3.6	V
Power Consumption		1.58	W
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%

## TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
<b>High-Speed I/Os</b>			
ip	20	CML input	Differential high-speed data/clock inputs with internal SE $50\Omega$ termination to $v_{cc}$
in	22		
icntp	2	CML input	Differential low-speed control inputs with internal SE $100\Omega$ termination to $v_{cc}$
icntn	4		
outp	10	CML output	Differential high-speed data/clock outputs with internal SE $50\Omega$ termination to $v_{cc}$ . Require external SE $50\Omega$ termination to $v_{cc}$
outn	8		
<b>Supply and Termination Voltages</b>			
Name	Description		Pin Number
vcc	Positive power supply (+3.3V or 0)		1, 3, 5, 7, 9, 11, 13, 14, 15, 16, 17, 19, 21, 23
vee	Negative power supply (0V or -3.3V)		6, 12, 18, 24



## ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<b>General Parameters</b>					
vee	-3.1	-3.3	-3.5	V	±6%
vcc		0.0		V	External ground
I <sub>vee</sub>		435		mA	
Power consumption		1435		mW	
Junction temperature	-40	25	125	°C	
<b>HS Input Data/Clock (ip/in)</b>					
Data Rate	DC		17	Gbps	
Frequency	DC		10	GHz	For clock signals
Swing	0.05		1.0	V	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	V	Must match for both inputs
<b>HS Output Data/Clock (outp/outn)</b>					
Data Rate	DC		17	Gbps	
Frequency	DC		10	GHz	For clock signals
Logic "1" level		vcc		V	
Logic "0" level		vcc-0.6		V	With external 50Ωm DC termination
Rise/Fall times	15	17	19	ps	20%-80%
Output Jitter			3	ps	Peak-to-peak
Duty cycle	45	50	55	%	For clock signal
<b>Output-to-Input Delay</b>					
Adjustment range		320		ps	For the full range of icntp/icntn control signals
Absolute delay stability	-4		4	ps	0-125°C
<b>Phase Shift Control port (icntp/icntn)</b>					
Bandwidth	DC		100	MHz	
SE voltage level	vcc-600		vcc	mV	Half control range when the opposite pin is at vcc
SE voltage level	vcc-1200		vcc	mV	Full control range when the opposite pin is at vcc-0.6V
Differential swing	0		1200	mV	Peak-peak, full control range
CM Level		vcc-(Diff. swing)/4		V	In differential mode

## PACKAGE INFORMATION

The chip die is housed in a standard 24-pin QFN package shown in Fig. 3. It is recommended that the center heat slug located on the back side of the package is soldered to the **vee** plain, which is ground for the positive supply or power for the negative supply. It will help dissipate heat generated by the chip during operation.

The part's identification label is ASNT5071-PQC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

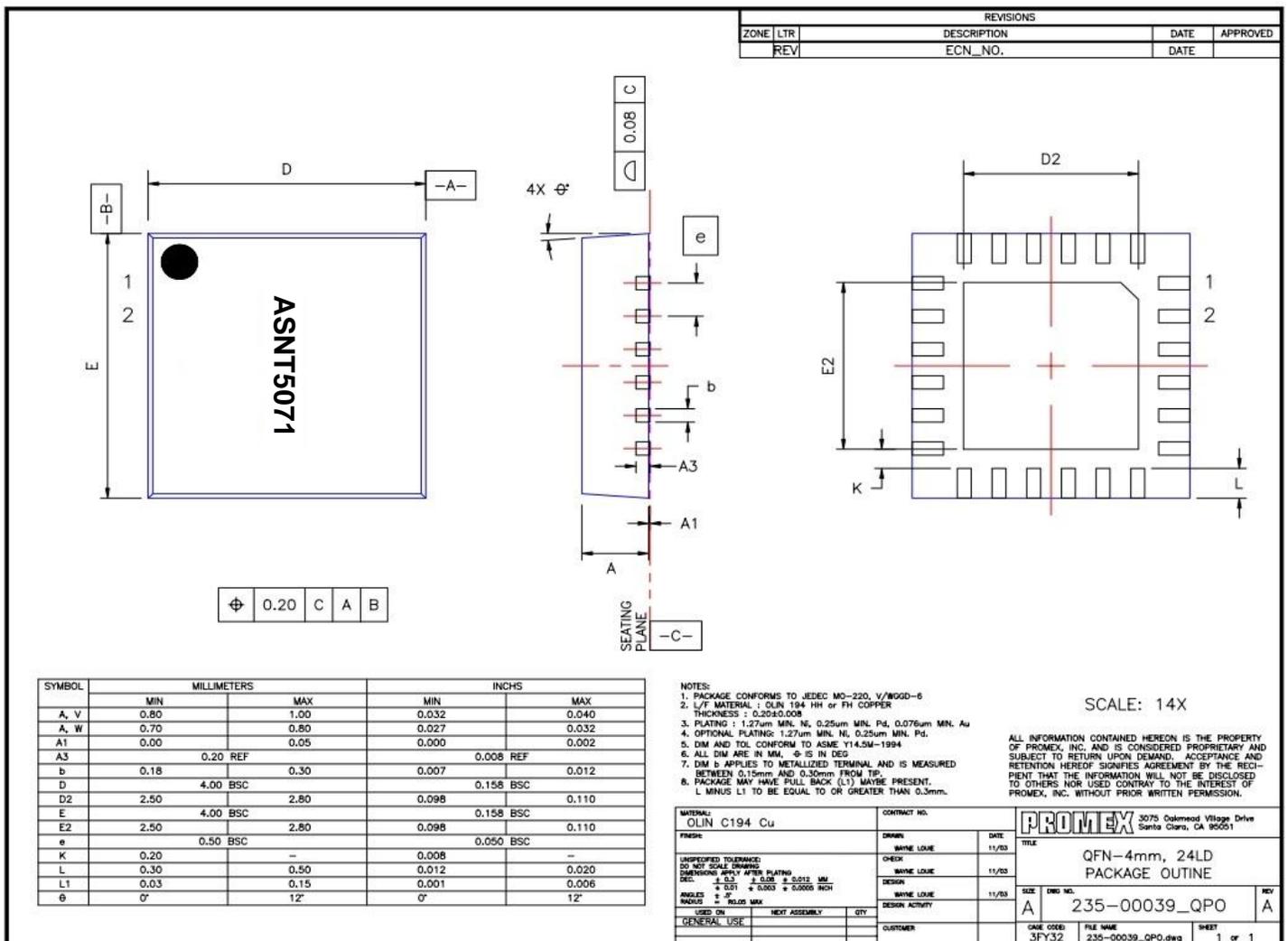


Fig. 3. QFN 24-Pin Package Drawing (All Dimensions in mm)



## REVISION HISTORY

Revision	Date	Changes
5.2.2	01-2020	Updated Package Information
5.1.2	07-2019	Updated Letterhead
5.1.1	06-2013	Revised description Corrected adjustment range Corrected delay control diagram Corrected electrical characteristics table
5.0.1	03-2013	Corrected title Revised package pin out drawing Revised functional block diagram Revised description Added delay graph Added power supply configuration Added absolute maximum ratings Revised terminal functions Revised electrical characteristics Revised package information Added mechanical drawing Format correction
4.0	10-2008	Revised electrical characteristics section Added packaging information section
3.0	06-2007	Revised electrical characteristics section
2.0	04-2007	Revised terminal functions section
1.0	01-2007	First release