

KSZ8863 Silicon Errata and Data Sheet Clarification

This document describes known silicon errata for the KSZ8863 family of devices. The silicon errata discussed in this document are for the silicon revisions listed in [Table 1](#). A summary of KSZ8863 silicon errata is provided in [Table 2](#).

TABLE 1: AFFECTED SILICON REVISIONS

Part Numbers	Silicon Revision
KSZ8863FLL, KSZ8863FLLI, KSZ8863MLL, KSZ8863MLLI, KSZ8863RLL, KSZ8863RLLI	A3

TABLE 2: SILICON ISSUE SUMMARY

Item Number	Silicon Issue Summary	Affected Silicon Revisions
1.	The rate for egress port rate limiting is incorrect when tag insertion is enabled	A3
2.	Switch won't start in I2C Master Mode	A3
3.	SMI management interface does not function if SPISN pin is not pulled high	A3
4.	Receiver error in 100BASE-TX mode following Soft Power Down	A3

Silicon Errata Issues

Module 1: The rate for egress port rate limiting is incorrect when tag insertion is enabled

DESCRIPTION

When tag insertion is enabled on an egress port and egress port rate limiting is turned on, the egress rate limit will be about twice the programmed value. When tag insertion is disabled, the egress rate limit is as programmed.

END USER IMPLICATIONS

The egress rate may exceed the programmed rate limit if tag insertion is enabled.

Work around

If both features are needed, use an egress rate setting of half the desired rate. However, even with this adjustment, the rate limit control may not be precise.

PLAN

This erratum will not be corrected in a future revision.

Module 2: Switch won't start in I²C Master Mode

DESCRIPTION

In I²C master mode, the switch reads register configurations from an attached EEPROM when exiting reset. In this mode, the Start Switch bit in Register 1 is cleared to '0', which disables the switch.

END USER IMPLICATIONS

After configuration from the external EEPROM, the switch is disabled and cannot be used since I²C master mode implies that there is no other external control of the switch registers.

Work around

When programming the EEPROM, set Register 78 (0x4E) bit 0 = '1'. This corrects the problem.

PLAN

This erratum will not be corrected in a future revision.

Module 3: SMI management interface does not function if SPISN pin is not pulled high

DESCRIPTION

If SPISN (pin 39) is left floating when the MIIM / SMI management mode is selected, the SMI interface will not work. This is due to the internal pull-down resistor on the SPISN pin. The MIIM management mode is unaffected.

END USER IMPLICATIONS

Registers cannot be accessed via SMI management interface if SPISN floats to a low level.

Work around

The problem is solved by pulling SPISN high with an external resistor to VDDIO. Use a resistor value between 1kΩ and 10kΩ.

PLAN

This erratum will not be corrected in a future revision.

Module 4: Receiver error in 100BASE-TX mode following Soft Power Down

DESCRIPTION

Some KSZ8863 devices may exhibit receiver errors after transitioning from Soft Power Down mode to Normal mode, as controlled by register 195 (0xC3) bits [1:0]. When exiting Soft Power Down mode, the receiver blocks may not start up properly, causing the PHY to miss data and exhibit erratic behavior. The problem may appear on either port 1 or port 2, or both ports. The problem occurs only for 100BASE-TX, not 10BASE-T.

END USER IMPLICATIONS

When the failure occurs, the following symptoms are seen on the affected port(s):

- The port is able to link
- LED0 blinks, even when there is no traffic
- The MIB counters indicate receive errors (Rx Fragments, Rx Symbol Errors, Rx CRC Errors, Rx Alignment Errors)
- Only a small fraction of packets is correctly received and forwarded through the switch. Most packets are dropped due to receive errors.

The failing condition cannot be corrected by the following:

- Removing and reconnecting the cable
- Hardware reset
- Software Reset and PCS Reset bits in register 67 (0x43)

Work around

The problem can be corrected by setting and then clearing the Port Power Down bits (registers 29 (0x1D) and 45 (0x2D), bit 3). This must be done separately for each affected port after returning from Soft Power Down Mode to Normal Mode. The following procedure will ensure no further issues due to this erratum.

To enter Soft Power Down Mode, set register 195 (0xC3), bits [1:0] = 10.

To exit Soft Power Down Mode, follow these steps:

1. Set register 195 (0xC3), bits [1:0] = 00 // Exit soft power down mode
2. Wait 1ms minimum
3. Set register 29 (0x1D), bit [3] = 1 // Enter PHY port 1 power down mode
4. Set register 29 (0x1D), bit [3] = 0 // Exit PHY port 1 power down mode
5. Set register 45 (0x2D), bit [3] = 1 // Enter PHY port 2 power down mode
6. Set register 45 (0x2D), bit [3] = 0 // Exit PHY port 2 power down mode

PLAN

This erratum will not be corrected in a future revision.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80000829A (04-10-19)	All	Converted to Microchip format.
	Module 4.	Added new erratum: Receiver error in 100BASE-TX mode following Soft Power Down

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