AN-1516
APPLICATION NOTE

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DC-Coupled, Single-Ended to Differential Conversion Using the AD8138 Low Distortion, Differential ADC Driver and AD7357 Dual, 4.2 MSPS, 14-Bit SAR ADC

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 provides dc-coupled, single-ended to differential conversion of a bipolar input signal to the AD7357 4.2 MSPS, 14-bit successive approximation register (SAR) analog-to-digital converter (ADC). This circuit has been designed to ensure maximum performance of the AD7357 by providing adequate settling time and low impedance.

CIRCUIT DESCRIPTION

Differential operation requires the V_{INx+} and V_{INx-} pins of the ADC to be driven simultaneously with two equal signals that are 180° out of phase and centered around the proper common-mode voltage. Because not all applications have a signal preconditioned for differential operation, there is often a need to perform a single-ended to differential conversion. An ideal method of applying differential drive to the AD7357 is to use a differential amplifier such as the AD8138. This device can be used as a single-ended to differential amplifier or as a differential to differential amplifier. The AD8138 also provides common-mode level shifting. Figure 1 shows how the AD8138 can be used as a single-ended to differential amplifier in a dc-coupled application. The positive and negative outputs of the AD8138 are connected to the respective inputs on the ADC through a pair of series resistors to minimize the loading effects of the switched capacitor inputs of the ADC. The architecture of the AD8138 results in outputs that are very highly balanced over a wide frequency range without requiring tightly matched external components. The single-ended to differential gain of the circuit in Figure 1 is equal to R_F/R_G, where $R_F = R_F1 = R_F2$ and $R_G = R_G1 = R_G2$.

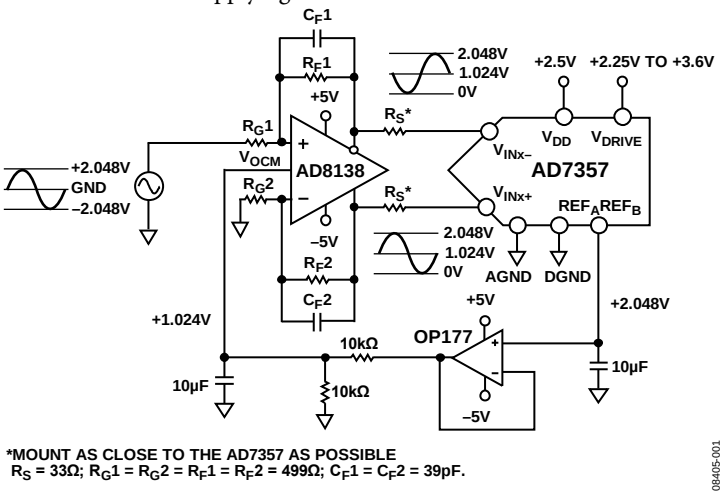

Figure 1. AD8138 as a DC-Coupled, Single-Ended to Differential Converter Driving the AD7357 Differential Inputs (Simplified Schematic)

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REVISION HISTORY

12/2017—Rev. B to Rev. C
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If the analog input source being used has zero impedance, all four resistors (RG1, RG2, RF1, and RF2) are the same, as shown in Figure 1. If the source has a 50 Ω impedance and a 50 Ω termination, for example, the value increase of RG2 is 25 Ω to balance this parallel impedance on the input and thus ensure that both the positive and negative analog inputs have the same gain. Impedance matching also requires a small increase in RF1 and RF2 to compensate for the gain loss caused by increasing RG1 and RG2. Complete analysis for the terminated source condition is found in the MT-076 Tutorial, Differential Driver Analysis and in the ADIDiffAmpCalc interactive design tool.

The AD7357 requires a driver that has a very fast settling time due to the very short acquisition time required to achieve 4.2 MSPS throughput with a serial interface. The track-and-hold amplifier on the front end of the AD7357 enters track mode on the rising edge of the 16th SCLK period during a conversion. The ADC driver must settle before the track-and-hold returns to hold (39 ns later for 4.2 MSPS throughput on the AD7357 using an 80 MHz SCLK). The AD8138 has a specified 16 ns settling time, which satisfies this requirement.

The voltage applied to the V_{OCM} pin of the AD8138 sets up the common-mode voltage. In Figure 1, V_{OCM} is connected to 1.024 V, which is a divided version of the internal 2.048 V reference on the AD7357. If the on-chip 2.048 V reference on the AD7357 is to be used elsewhere in a system (as shown in Figure 1), the output from REF_A or REF_B must first be buffered. The OP177 features high precision performance, making it a perfect reference buffer choice.

Note that in Figure 1, the AD8138 operates on dual 5 V, supplies, whereas the AD7357 is specified for power supply voltages of 2.5 V to 3.6 V. Care must be taken to ensure that the input maximum input voltage limits of the AD7357 are not exceeded during transient or power-on conditions (see the MT-036 Tutorial, *Op Amp Output Phase-Reversal and Input Over-Voltage Protection*).

In addition, the circuit must be constructed on a multilayer printed circuit board (PCB) with a large area ground plane. Proper layout, grounding, and decoupling techniques must be used to achieve optimum performance (see the MT-031 Tutorial, Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"; the MT-101 Tutorial, *Decoupling Techniques*; and the EVAL-AD7357 layout).

COMMON VARIATIONS

The OP07D, an ultralow offset voltage op amp, is a lower cost alternative to the OP177. It offers similar performance with the exception of the input offset voltage (V_{OS}) specification. Alternatively, the AD8628 or the AD8638 offers very high precision with very low drift with time and temperature.

REFERENCES

ADIDiffAmpCalc

Ardizonni, John and Jonathan Pearson. "Rules of the Road for High-Speed Differential ADC Drivers." *Analog Dialogue.* May 2009.

Kester, Walt, Bryant, James, and Byrne Mike. MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND."* Analog Devices.

MT-036 Tutorial, *Op Amp Output Phase-Reversal and Input Over-Voltage Protection.* Analog Devices.

MT-074 Tutorial, *Differential Drivers for Precision ADCs.* Analog Devices.

MT-075 Tutorial, *Differential Drivers for High Speed ADCs Overview.* Analog Devices.

MT-076 Tutorial, *Differential Driver Analysis.* Analog Devices.

MT-101 Tutorial, *Decoupling Techniques.* Analog Devices.