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ON Semiconductor®

# FDP8030L/FDB8030L

## N-Channel Logic Level PowerTrench® MOSFET

### General Description

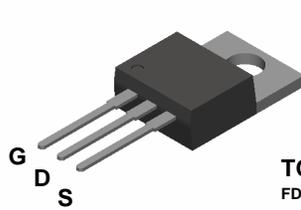
This N-Channel Logic level MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETS feature faster switching and lower gate charge than other MOSFETS with comparable  $R_{DS(on)}$  specifications.

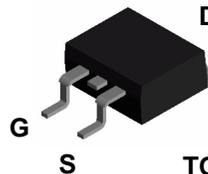
The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

### Features

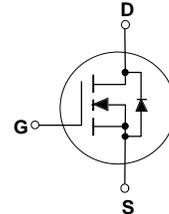
- 80 A, 30 V.  $R_{DS(on)} = 0.0035 \Omega @ V_{GS} = 10 V$   
 $R_{DS(on)} = 0.0045 \Omega @ V_{GS} = 4.5 V$
- Critical DC electrical parameters specified at elevated temperature
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor
- High performance trench technology for extremely low  $R_{DS(on)}$
- 175°C maximum junction temperature rating



TO-220  
FDP Series



TO-263AB  
FDB Series



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage	30	V
V <sub>GSS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current – Continuous (Note 1)	80	A
	– Pulsed (Note 1)	300	
P <sub>D</sub>	Total Power Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	187	W
		1.25	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-65 to +175	°C
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275	°C

### Thermal Characteristics

R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	0.8	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	62.5	°C/W

FDP8030L/FDB8030L

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Drain-Source Avalanche Ratings (Note 1)**

$W_{DSS}$	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 20\text{ V}, I_D = 80\text{ A}$			1500	mJ
$I_{AR}$	Maximum Drain-Source Avalanche Current				80	A

**Off Characteristics**

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		23		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

**On Characteristics (Note 2)**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.5	2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 80\text{ A}, T_J = 125^\circ\text{C}$		3.1	3.5	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 70\text{ A}$		4.0	5.6	
				3.6	4.5	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}$	60			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 80\text{ A}$		170		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$		10500		pF
$C_{oss}$	Output Capacitance	$f = 1.0\text{ MHz}$		2700		pF
$C_{riss}$	Reverse Transfer Capacitance			1650		pF

**Switching Characteristics (Note 2)**

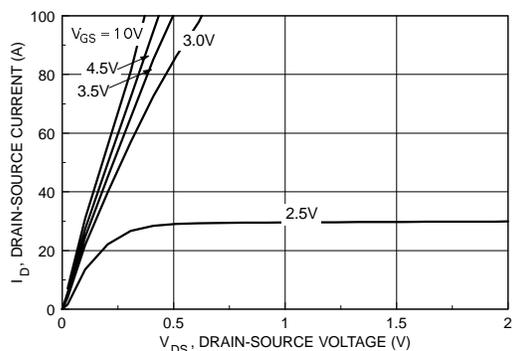
$t_{D(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 50\text{ A},$		20	35	ns
$t_r$	Turn-On Rise Time	$V_{GS} = 4.5\text{ V}, R_{GEN} = 10\ \Omega$		185	225	ns
$t_{D(off)}$	Turn-Off Delay Time	$R_{GS} = 10\ \Omega$		160	200	ns
$t_f$	Turn-Off Fall Time			200	240	ns
$Q_g$	Total Gate Charge	$V_{DS} = 15\text{ V},$		120	170	nC
$Q_{gs}$	Gate-Source Charge	$I_D = 80\text{ A}, V_{GS} = 5\text{ V}$		27		nC
$Q_{gd}$	Gate-Drain Charge			48		nC

**Drain-Source Diode Characteristics and Maximum Ratings**

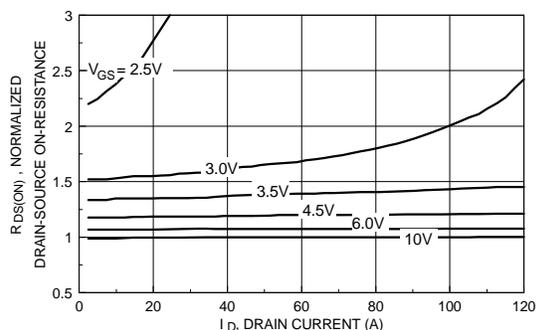
$I_S$	Maximum Continuous Drain-Source Diode Forward Current (Note 1)				80	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current (Note 1)				300	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 80\text{ A}$ (Note 1)		1	1.3	V

**Notes:**1. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

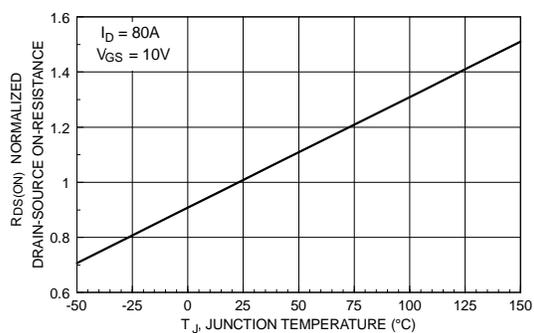
## Typical Characteristics



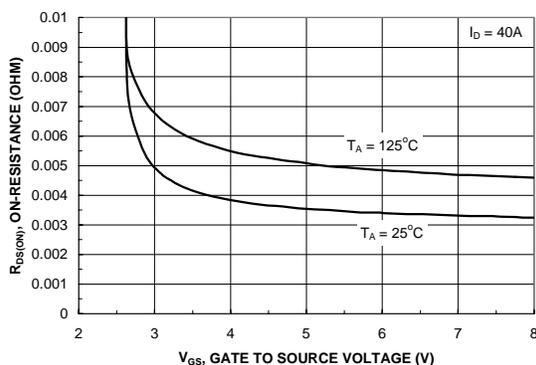
**Figure 1. On-Region Characteristics.**



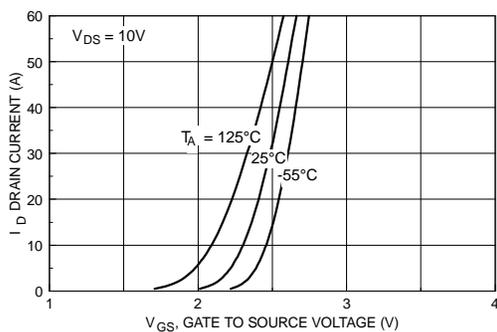
**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**



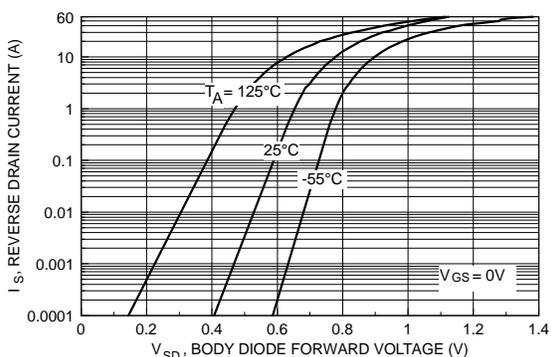
**Figure 3. On-Resistance Variation with Temperature.**



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**



**Figure 5. Transfer Characteristics.**



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics

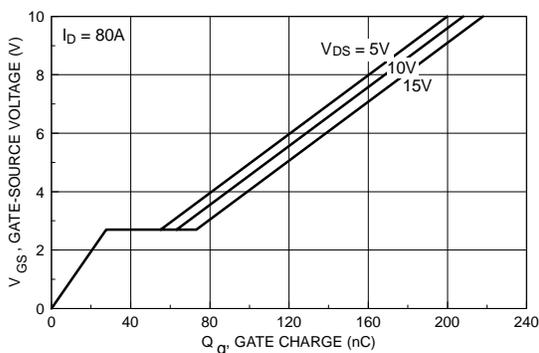


Figure 7. Gate Charge Characteristics.

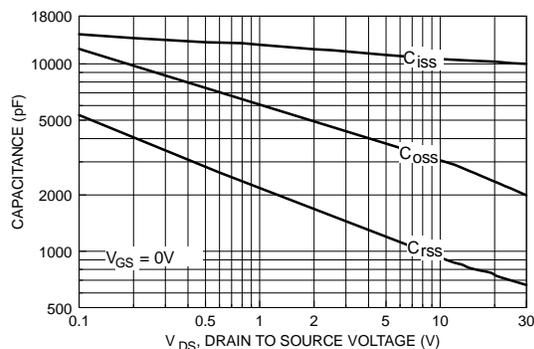


Figure 8. Capacitance Characteristics.

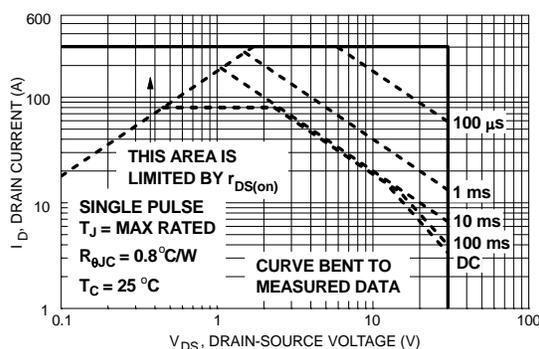


Figure 9. Maximum Safe Operating Area.

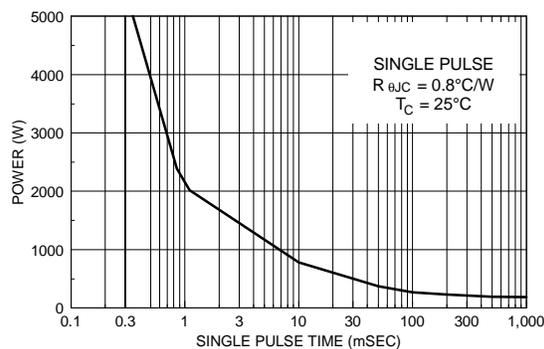


Figure 10. Single Pulse Maximum Power Dissipation.

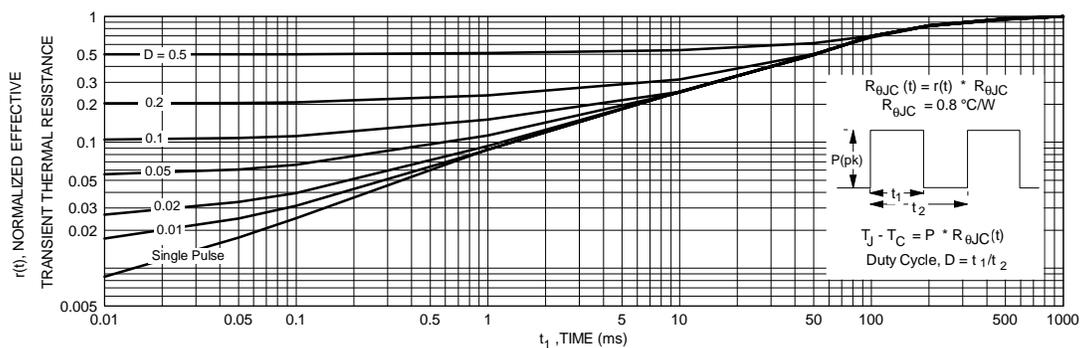


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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