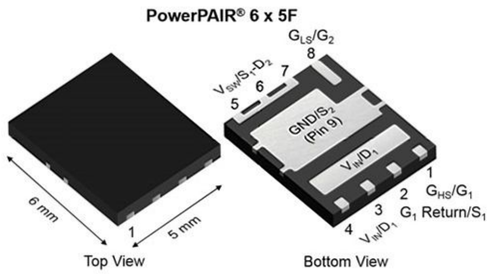
Dual N-Channel 25 V (D-S) MOSFET with Schottky Diode



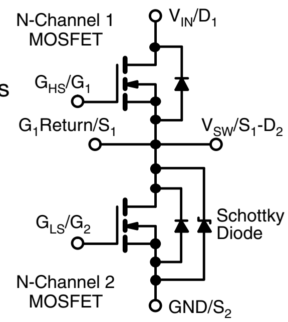
FEATURES

- TrenchFET® Gen IV power MOSFET
- SkyFET® low side MOSFET with integrated Schottky
- G_1 return/S_1 pin for enhancing high side driving
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- CPU core power
- Computer / server peripherals
- POL
- Synchronous buck converter
- Telecom DC/DC



PRODUCT SUMMARY

	CHANNEL-1	CHANNEL-2
V_{DS} (V)	25	25
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.00380	0.00090
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.00620	0.00150
Q_g typ. (nC)	6.6	31
I_D (A) [a]	40	60
Configuration	Dual	

ORDERING INFORMATION

Package	PowerPAIR 6 x 5F
Lead (Pb)-free and halogen-free	SiZF914DT-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	CHANNEL-1	CHANNEL-2	UNIT
Drain-source voltage		V_{DS}	25	25	V
Gate-source voltage		V_{GS}	+20, -16	+16, -12	V
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	40 [a]	60 [a]	A
	T_C = 70 °C		40 [a]	60 [a]	
	T_A = 25 °C		23.5 [b, c]	52 [b, c]	
	T_A = 70 °C		19 [b, c]	42 [b, c]	
Pulsed drain current (t = 100 μs)		I_{DM}	130	110	
Continuous source-drain diode current	T_C = 25 °C	I_S	22	60 [a]	
	T_A = 25 °C		2.8 [b, c]	6.7 [b, c]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	20	34	
Single pulse avalanche energy		E_{AS}	20	58	mJ
Maximum power dissipation	T_C = 25 °C	P_D	26.6	60	W
	T_C = 70 °C		17	38	
	T_A = 25 °C		3.4 [b, c]	4 [b, c]	
	T_A = 70 °C		2.2 [b, c]	2.6 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150		°C
Soldering recommendations (peak temperature) [d, e]			260		

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	CHANNEL-1		CHANNEL-2		UNIT
			TYP.	MAX.	TYP.	MAX.	
Maximum junction-to-ambient [b, f]	t ≤ 10 s	R_{thJA}	30	37	25	31	°C/W
Maximum junction-to-case (source)	Steady state	R_{thJC}	3.8	4.7	1.7	2.1	

Notes

a. Package limited
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s
d. See solder profile (www.vishay.com/doc?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
f. Maximum under steady state conditions is 77 °C/W for channel-1 and 68 °C/W for channel-2

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	Ch-1	25	-	-	V
			Ch-2	25	-	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	Ch-1	1.1	-	2.4	
			Ch-2	1.1	-	2.2	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = +20 V, -16 V	Ch-1	-	-	± 100	nA
		V_{DS} = 0 V, V_{GS} = +16 V, -12 V	Ch-2	-	-	± 100	
Zero Gate voltage drain current	I_{DSS}	V_{DS} = 25 V, V_{GS} = 0 V	Ch-1	-	-	1	μA
			Ch-2	-	30	350	
		V_{DS} = 25 V, V_{GS} = 0 V, T_J = 55 °C	Ch-1	-	-	5	
			Ch-2	-	200	3000	
On-state drain current [b]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	Ch-1	20	-	-	A
			Ch-2	20	-	-	
Drain-source on-state resistance [b]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A	Ch-1	-	0.00270	0.00380	Ω
		V_{GS} = 10 V, I_D = 10 A	Ch-2	-	0.00060	0.00090	
		V_{GS} = 4.5 V, I_D = 5 A	Ch-1	-	0.00410	0.00620	
		V_{GS} = 4.5 V, I_D = 5 A	Ch-2	-	0.00095	0.00150	
Forward transconductance [b]	g_{fs}	V_{DS} = 10 V, I_D = 20 A	Ch-1	-	45	-	S
		V_{DS} = 10 V, I_D = 20 A	Ch-2		105	-	
Dynamic [a]							
Input capacitance	C_{iss}	Channel-1 V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz Channel-2 V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	Ch-1	-	1050	-	pF
			Ch-2	-	4670	-	
Output capacitance	C_{oss}		Ch-1	-	510	-	
			Ch-2	-	1650	-	
Reverse transfer capacitance	C_{rss}		Ch-1	-	47	-	
			Ch-2	-	370	-	
C_{rss}/C_{iss} ratio			Ch-1	-	0.036	0.072	
			Ch-2		0.062	0.125	
Total gate charge	Q_g	V_{DS} = 10 V, V_{GS} = 10 V, I_D = 10 A	Ch-1	-	14	21	nC
			Ch-2	-	65	98	
		Channel-1 V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 10 A Channel-2 V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 10 A	Ch-1		6.6	10	
			Ch-2	-	31	47	
Gate-source charge	Q_{gs}		Ch-1	-	3.2	-	
			Ch-2	-	10.2	-	
Gate-drain charge	Q_{gd}		Ch-1	-	1.2	-	
			Ch-2	-	6.4	-	
Output charge	Q_{oss}	V_{DS} = 10 V, V_{GS} = 0 V	Ch-1	-	7.5	-	
			Ch-2	-	27	-	
Gate resistance	R_g	f = 1 MHz	Ch-1	0.2	1	2	Ω
			Ch-2	0.1	0.3	0.6	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Dynamic [a]							
Turn-on delay time	$t_{d(on)}$	Channel-1 V_{DD} = 10 V, R_L = 2 Ω $I_D \cong$ 5 A, V_{GEN} = 4.5 V, R_g = 1 Ω Channel-2 V_{DD} = 10 V, R_L = 2 Ω $I_D \cong$ 5 A, V_{GEN} = 4.5 V, R_g = 1 Ω	Ch-1	-	20	40	ns
			Ch-2	-	32	60	
Rise time	t_r		Ch-1	-	50	100	
			Ch-2	-	60	120	
Turn-off delay time	$t_{d(off)}$		Ch-1	-	15	30	
			Ch-2	-	45	90	
Fall time	t_f		Ch-1	-	10	20	
			Ch-2	-	15	30	
Turn-on delay time	$t_{d(on)}$	Channel-1 V_{DD} = 10 V, R_L = 2 Ω $I_D \cong$ 5 A, V_{GEN} = 10 V, R_g = 1 Ω Channel-2 V_{DD} = 10 V, R_L = 2 Ω $I_D \cong$ 5 A, V_{GEN} = 10 V, R_g = 1 Ω	Ch-1	-	12	25	
			Ch-2	-	16	30	
Rise time	t_r		Ch-1	-	5	10	
			Ch-2	-	30	60	
Turn-off delay time	$t_{d(off)}$		Ch-1	-	20	40	
			Ch-2	-	40	80	
Fall time	t_f		Ch-1	-	5	10	
			Ch-2	-	6	15	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	T_C = 25 °C	Ch-1	-	-	22	A
			Ch-2	-	-	60	
Pulse diode forward current [a]	I_{SM}		Ch-1	-	-	130	
			Ch-2	-	-	110	
Body diode voltage	V_{SD}	I_S = 5 A, V_{GS} = 0 V	Ch-1	-	0.8	1.2	V
		I_S = 3 A, V_{GS} = 0 V	Ch-2	-	0.38	0.6	
Body diode reverse recovery time	t_{rr}	Channel-1 I_F = 5 A, di/dt = 100 A/μs, T_J = 25 °C Channel-2 I_F = 5 A, di/dt = 100 A/μs, T_J = 25 °C	Ch-1	-	36	70	ns
			Ch-2	-	66	130	
Body diode reverse recovery charge	Q_{rr}		Ch-1	-	36	50	nC
			Ch-2	-	72	150	
Reverse recovery fall time	t_a		Ch-1	-	20	-	ns
			Ch-2	-	30	-	
Reverse recovery rise time	t_b		Ch-1	-	16	-	
			Ch-2	-	36	-	

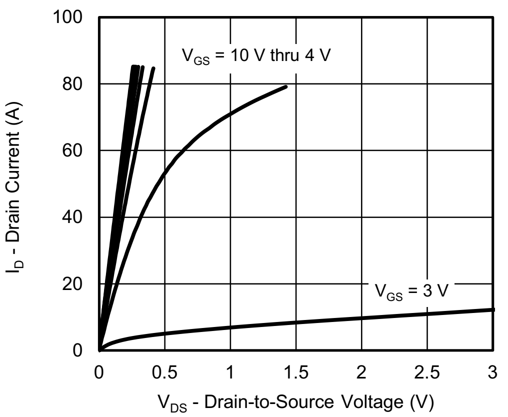
Notes

a. Guaranteed by design, not subject to production testing

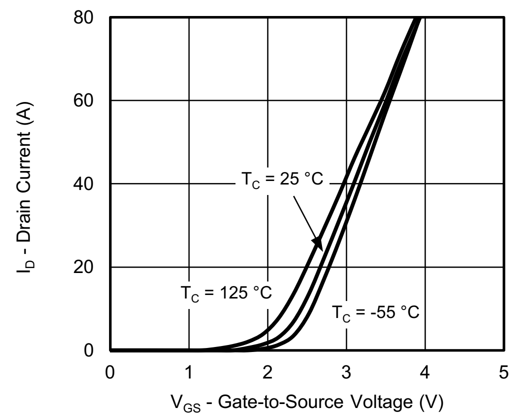
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

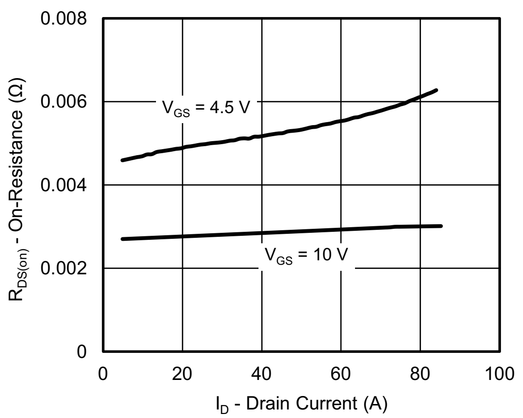
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



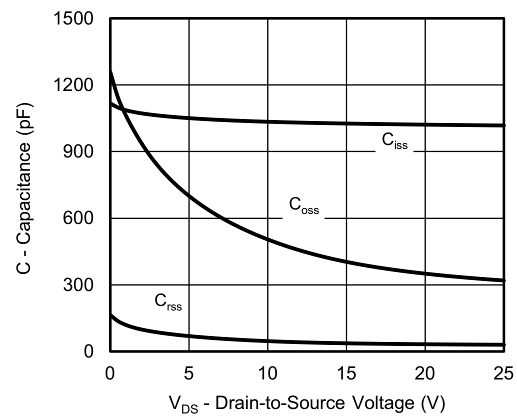
Output Characteristics



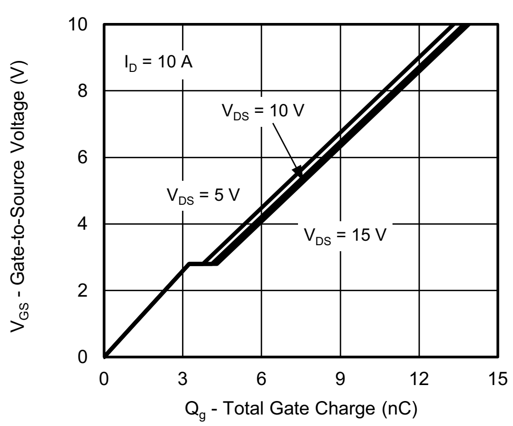
Transfer Characteristics



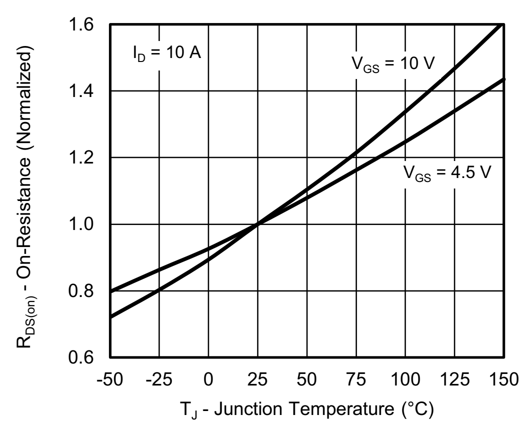
On-Resistance vs. Drain Current



Capacitance

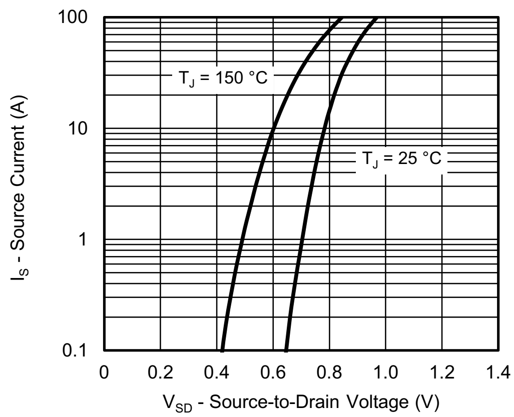


Gate Charge

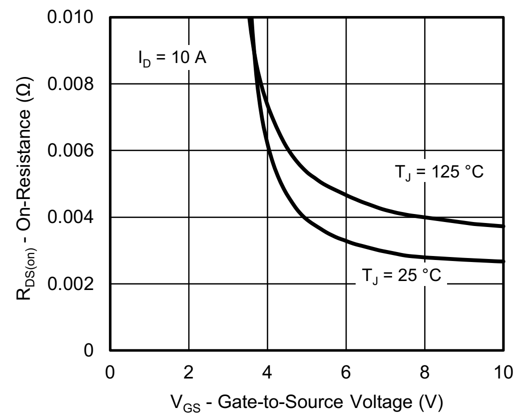


On-Resistance vs. Junction Temperature

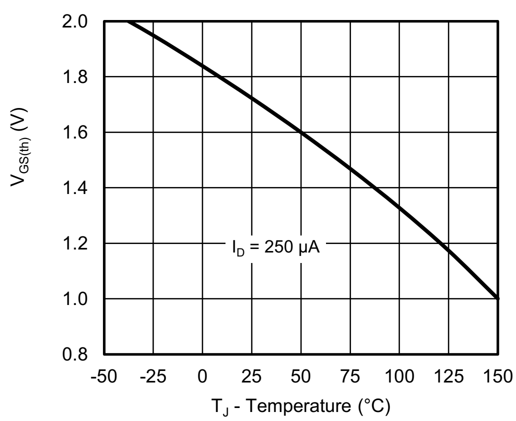
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



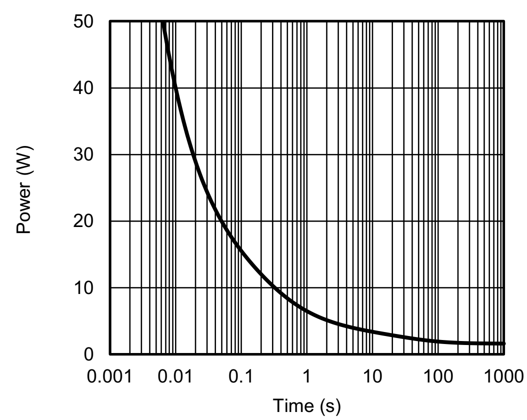
Source-Drain Diode Forward Voltage



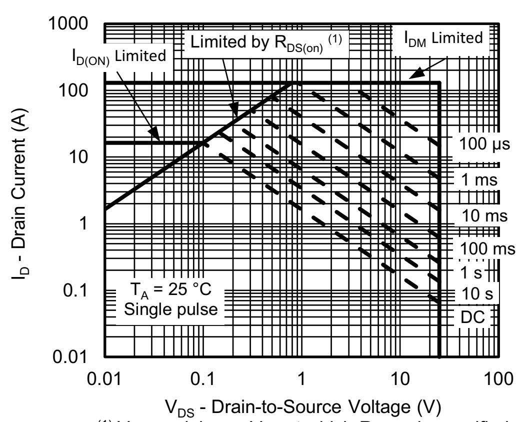
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



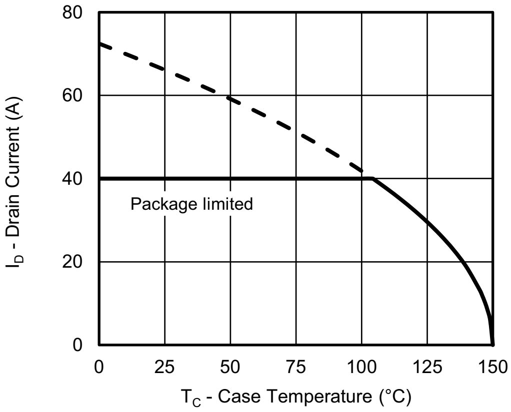
Single Pulse Power, Junction-to-Ambient



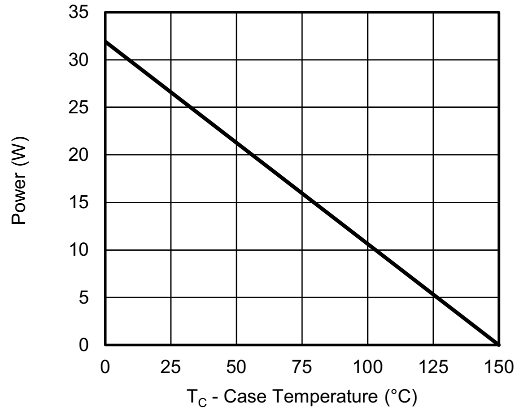
(1) V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]

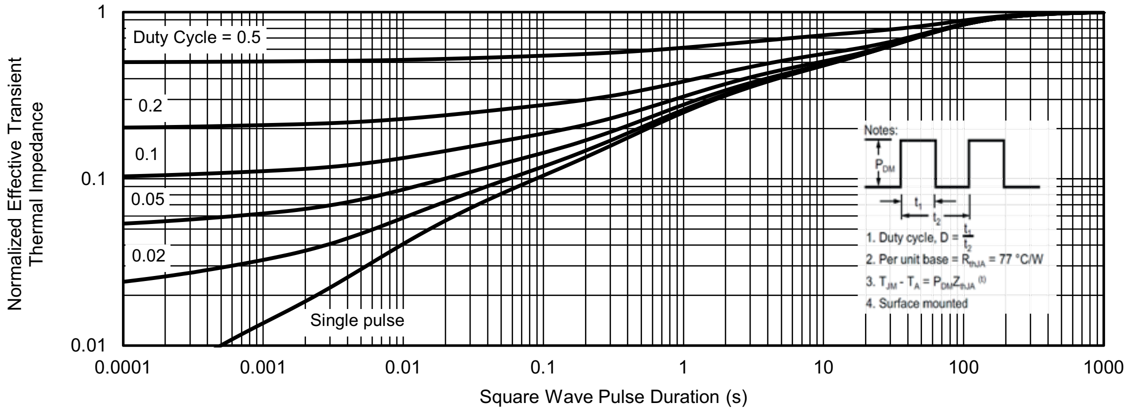


Power, Junction-to-Case

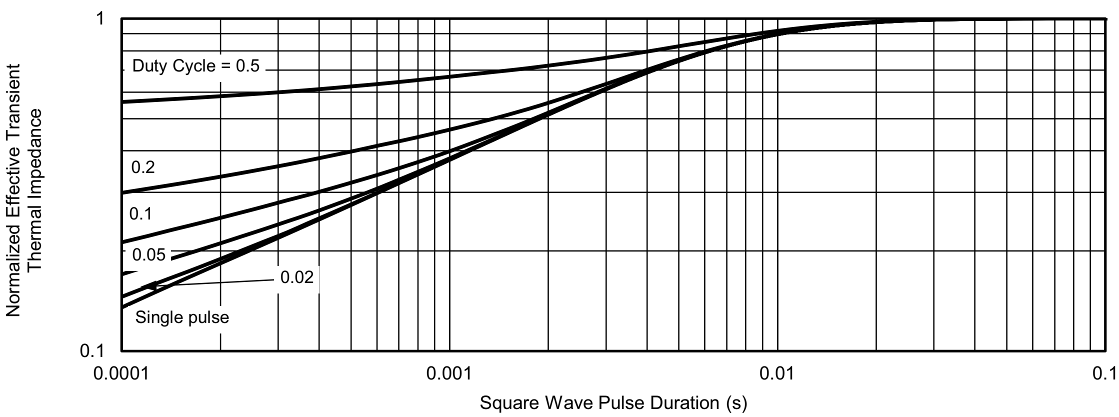
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

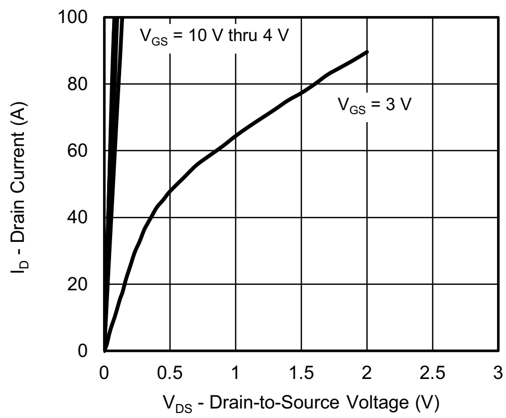


Normalized Thermal Transient Impedance, Junction-to-Ambient

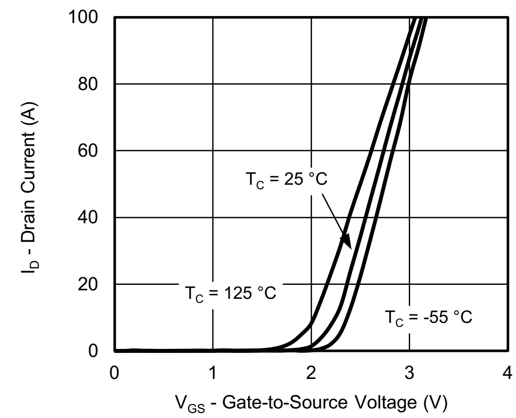


Normalized Thermal Transient Impedance, Junction-to-Case

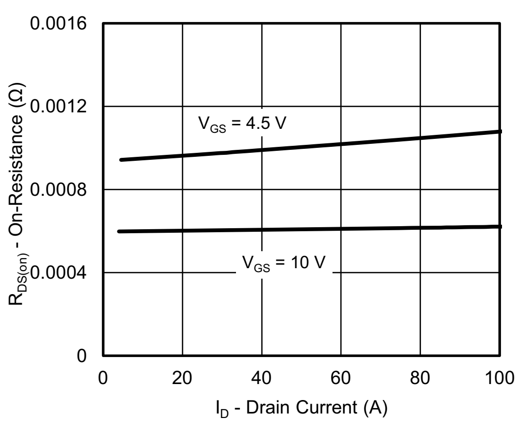
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



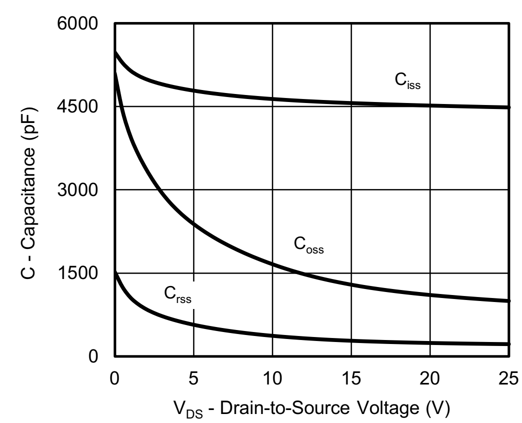
Output Characteristics



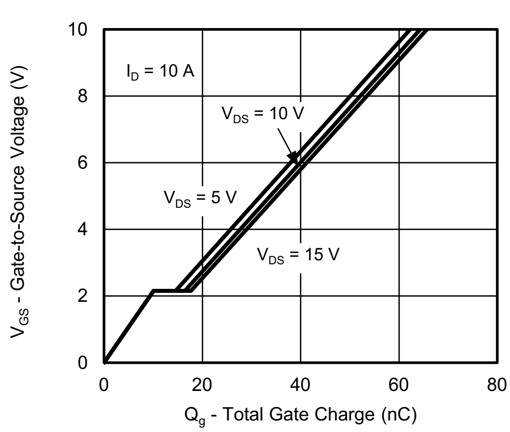
Transfer Characteristics



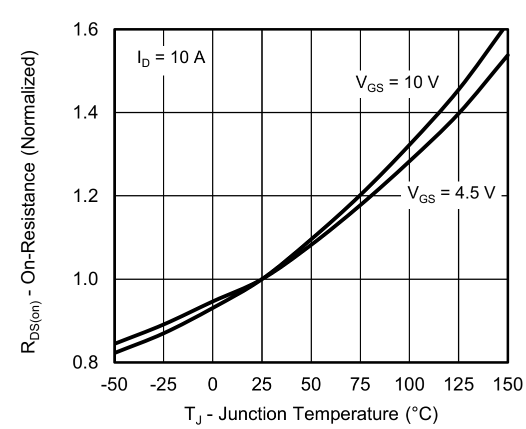
On-Resistance vs. Drain Current



Capacitance

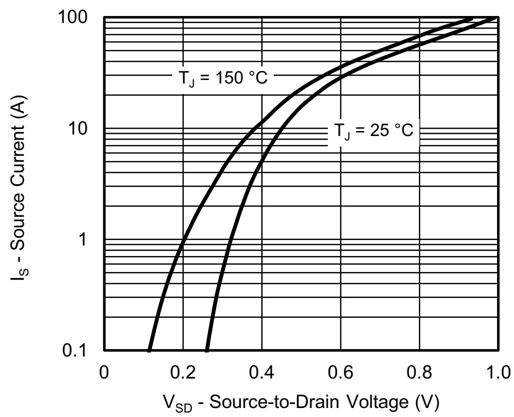


Gate Charge

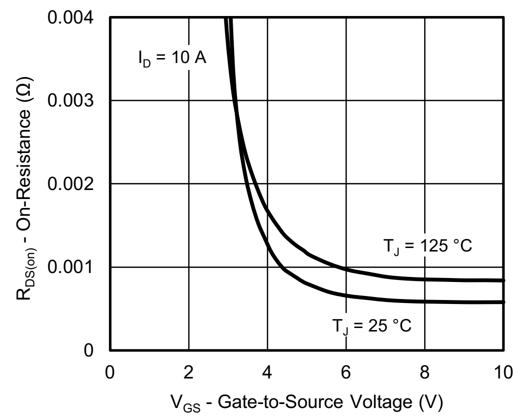


On-Resistance vs. Junction Temperature

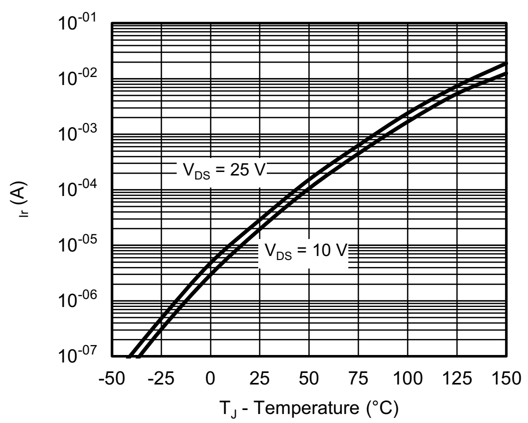
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



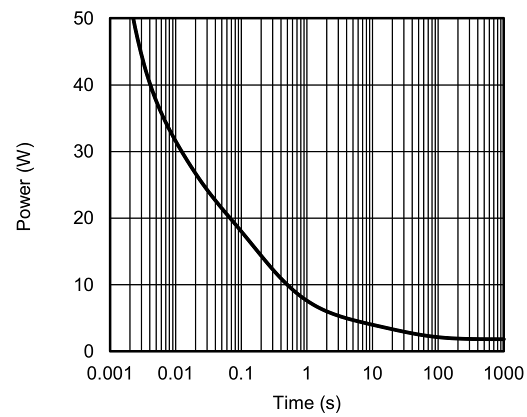
Source-Drain Diode Forward Voltage



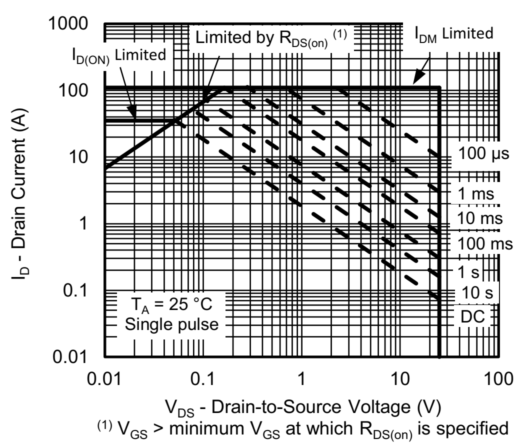
On-Resistance vs. Gate-to-Source Voltage



Reverse Current (Schottky)

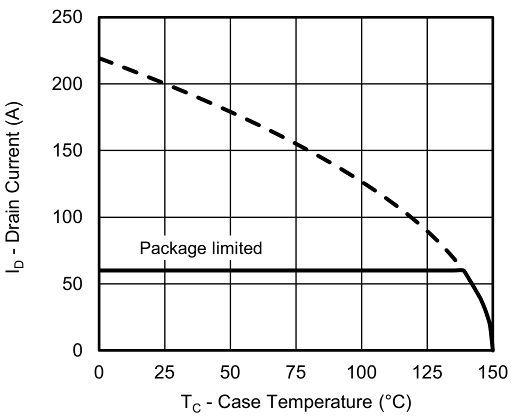


Single Pulse Power, Junction-to-Ambient

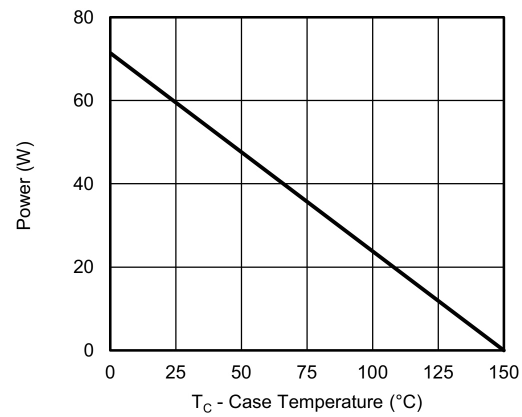


Safe Operating Area, Junction-to-Ambient

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]

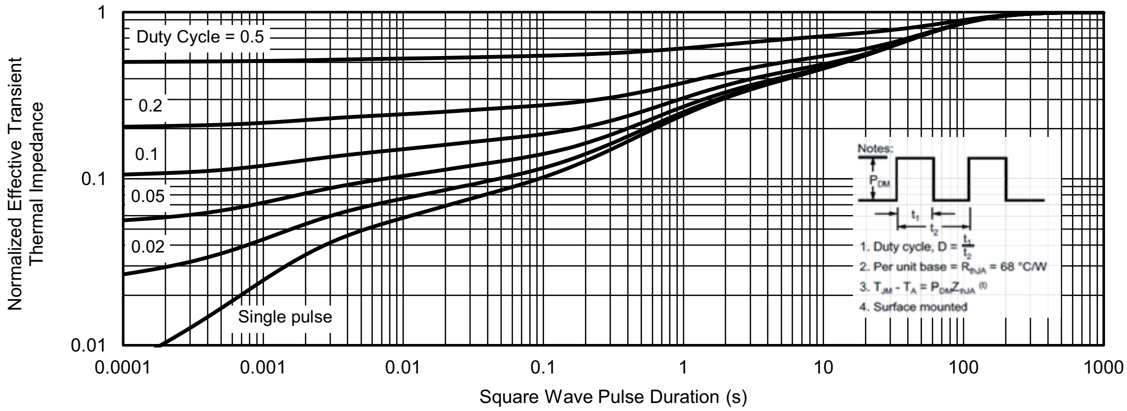


Power, Junction-to-Case

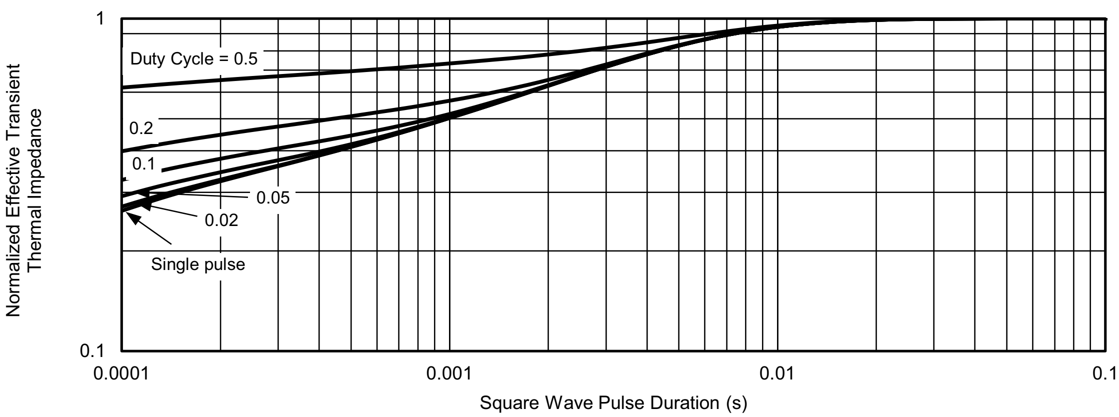
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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