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SEMICONDUCTOR TM

NDS9925A Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

SO-8 N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 4.5 A, 20 V. $R_{DS(ON)} = 0.060 \ \Omega \ @ V_{GS} = 4.5 \ V$ $R_{DS(ON)} = 0.075 \ \Omega \ @ V_{GS} = 2.7 \ V.$
- High density cell design for extremely low R_{DS(ON)}.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.







Absolute Maximum Ratings $T_A = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	NDS9925A	Units
V _{DSS}	Drain-Source Voltage	20	V
V _{GSS}	Gate-Source Voltage	±8	V
l _D	Drain Current - Continuous (Note	1a) 4.5	A
	- Pulsed	15	
P _D	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1	a) 1.6	
	(Note 1	b) 1	
	(Note 1	c) 0.9	
T _J ,T _{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMA	L CHARACTERISTICS		-
R _{eja}	Thermal Resistance, Junction-to-Ambient (Note 1a	a) 78	°C/W
R _{eJC}	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

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Symbol	Parameter	Conditions	Min	Тур	Max	Units
OFF CHA	RACTERISTICS					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{gg} = 0 V, I_{D} = 250 \mu A$	20			V
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16 V, V_{GS} = 0 V$			1	μA
	Gate - Body Leakage, Forward	$V_{gg} = 8 V, V_{Dg} = 0 V$			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	$V_{gg} = -8 V, V_{Dg} = 0 V$			-100	nA
ON CHAR	ACTERISTICS (Note 2)					•
V _{GS(th)}	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}, \ I_{\text{D}} = 250 \ \mu\text{A}$	0.4		1	V
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{gg} = 4.5 \text{ V}, \ I_{p} = 4.5 \text{ A}$			0.06	Ω
		$V_{gg} = 2.7 V, I_{D} = 4 A$			0.075	
I _{D(on)}	On-State Drain Current	$V_{GS} = 4.5 \text{ V}, V_{DS} = 5 \text{ V}$	15			Α
DRAIN-SO	URCE DIODE CHARACTERISTICS AND MA	XIMUM RATINGS				
l _s	Maximum Continuous Drain-Source Diode Forward Current				1.3	А
V _{SD}	Drain-Source Diode Forward Voltage	$V_{gs} = 0 V, I_s = 1.3 A$ (Note 2)			1.2	V

Notes :

1. R_{gAM} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{gAC} is guaranteed by design while $\mathrm{R}_{_{\theta CA}}$ is determined by the user's board design.



a. 78°C/W on a 0.5 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper 2. Pulse Test: Pulse Width \leq 300µs, Duty Cycle \leq 2.0%.



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