

# MCR72-3, MCR72-6, MCR72-8

## Sensitive Gate Silicon Controlled Rectifiers Reverse Blocking Thyristors

Designed for industrial and consumer applications such as temperature, light and speed control; process and remote controls; warning systems; capacitive discharge circuits and MPU interface.

### Features

- Center Gate Geometry for Uniform Current Density
- All Diffused and Glass-Passivated Junctions for Parameter Uniformity and Stability
- Small, Rugged Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Low Trigger Currents, 200  $\mu$ A Maximum for Direct Driving from Integrated Circuits
- These are Pb-Free Devices\*

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) ( $T_J = -40$ to $110^\circ\text{C}$ , Sine Wave, 50 Hz to 60 Hz)	$V_{DRM}$ , $V_{RRM}$	100 400 600	V
On-State RMS Current ( $180^\circ$ Conduction Angles; $T_C = 83^\circ\text{C}$ )	$I_{T(RMS)}$	8.0	A
Peak Non-Repetitive Surge Current (1/2 Cycle, 60 Hz, $T_J = 110^\circ\text{C}$ )	$I_{TSM}$	100	A
Circuit Fusing Considerations ( $t = 8.3$ ms)	$I^2t$	40	$\text{A}^2\text{s}$
Forward Peak Gate Voltage ( $t \leq 10$ $\mu\text{s}$ , $T_C = 83^\circ\text{C}$ )	$V_{GM}$	$\pm 5.0$	V
Forward Peak Gate Current ( $t \leq 10$ $\mu\text{s}$ , $T_C = 83^\circ\text{C}$ )	$I_{GM}$	1.0	A
Forward Peak Gate Power ( $t \leq 10$ $\mu\text{s}$ , $T_C = 83^\circ\text{C}$ )	$P_{GM}$	5.0	W
Average Gate Power ( $t = 8.3$ ms, $T_C = 83^\circ\text{C}$ )	$P_{G(AV)}$	0.75	W
Operating Junction Temperature Range	$T_J$	$-40$ to $+110$	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	$-40$ to $+150$	$^\circ\text{C}$
Mounting Torque	–	8.0	in. lb.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1.  $V_{DRM}$  and  $V_{RRM}$  for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

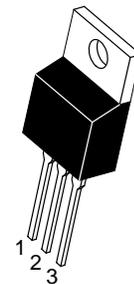
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



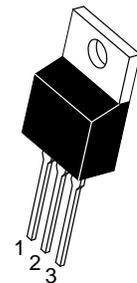
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SCRs  
8 AMPERES RMS  
100 thru 600 VOLTS



TO-220AB  
CASE 221A-07  
STYLE 3



TO-220AB  
CASE 221A-09  
STYLE 3

### PIN ASSIGNMENT

1	Cathode
2	Anode
3	Gate
4	Anode

### MARKING AND ORDERING INFORMATION

See detailed marking, ordering, and shipping information in the package dimensions section on page 4 of this data sheet.

# MCR72-3, MCR72-6, MCR72-8

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.2	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	60	$^{\circ}C/W$
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Secs	$T_L$	260	$^{\circ}C$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^{\circ}C$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Peak Repetitive Forward or Reverse Blocking Current (Note 2) ( $V_{AK} = \text{Rated } V_{DRM} \text{ or } V_{RRM}; R_{GK} = 1 \text{ k}\Omega$ )	$I_{DRM}, I_{RRM}$	-	-	10	$\mu A$
		-	-	500	$\mu A$
High Logic Level Supply Current from $V_{CC}$	$I_{CCH}$	4	4	$\mu A$	$\mu A$

### ON CHARACTERISTICS

Peak Forward On-State Voltage ( $I_{TM} = 16 \text{ A Peak, Pulse Width } \leq 1 \text{ ms, Duty Cycle } \leq 2\%$ )	$V_{TM}$	-	1.7	2.0	V
Gate Trigger Current (Continuous dc) (Note 3) ( $V_D = 12 \text{ V, } R_L = 100 \Omega$ )	$I_{GT}$	-	30	200	$\mu A$
Gate Trigger Voltage (Continuous dc) (Note 3) ( $V_D = 12 \text{ V, } R_L = 100 \Omega$ )	$V_{GT}$	-	0.5	1.5	V
Gate Non-Trigger Voltage ( $V_D = 12 \text{ Vdc, } R_L = 100 \Omega, T_J = 110^{\circ}C$ )	$V_{GD}$	0.1	-	-	V
Holding Current ( $V_D = 12 \text{ V, Initiating Current} = 200 \text{ mA, } R_{GK} = 1 \text{ k}\Omega$ )	$I_H$	-	-	6.0	mA
Gate Controlled Turn-On Time ( $V_D = \text{Rated } V_{DRM}, I_{TM} = 16 \text{ A, } I_G = 2 \text{ mA}$ )	$t_{gt}$	-	1.0	-	$\mu s$

### DYNAMIC CHARACTERISTICS

Critical Rate-of-Rise of Off-State Voltage ( $V_D = \text{Rated } V_{DRM}, R_{GK} = 1 \text{ k}\Omega, T_J = 110^{\circ}C, \text{ Exponential Waveform}$ )	$dv/dt$	-	10	-	$V/\mu s$
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Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Ratings apply for negative gate voltage or  $R_{GK} = 1 \text{ k}\Omega$ . Devices shall not have a positive gate voltage concurrently with a negative voltage on the anode. Devices should not be tested with a constant current source for forward and reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.
- $R_{GK}$  current not included in measurement.

# MCR72-3, MCR72-6, MCR72-8

## Voltage Current Characteristic of SCR

Symbol	Parameter
$V_{DRM}$	Peak Repetitive Off State Forward Voltage
$I_{DRM}$	Peak Forward Blocking Current
$V_{RRM}$	Peak Repetitive Off State Reverse Voltage
$I_{RRM}$	Peak Reverse Blocking Current
$V_{TM}$	Peak On State Voltage
$I_H$	Holding Current

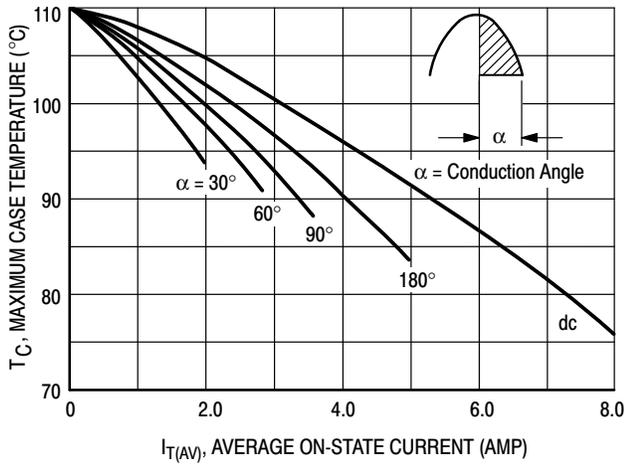
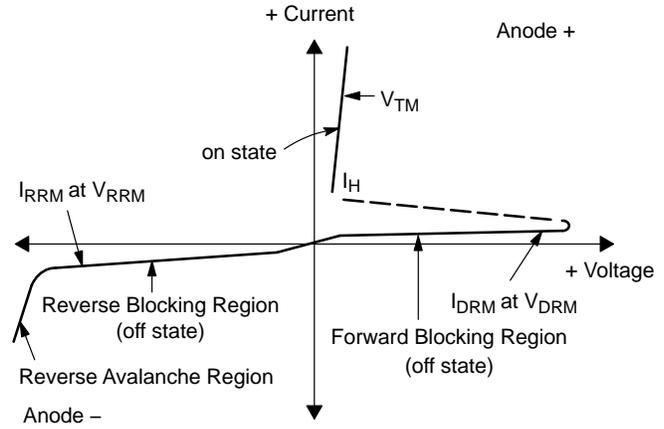


Figure 1. Average Current Derating

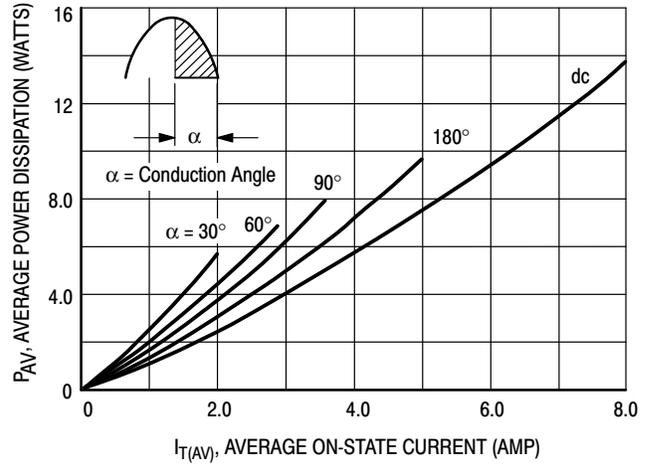


Figure 2. On-State Power Dissipation

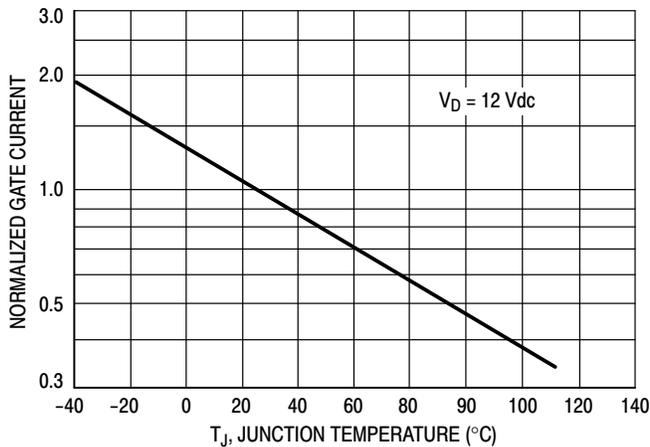


Figure 3. Normalized Gate Current

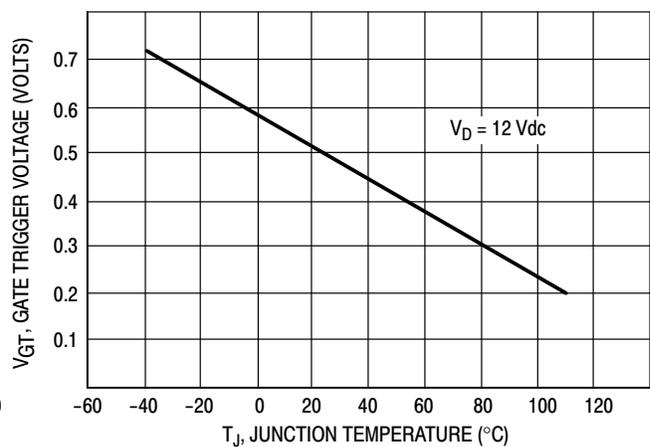
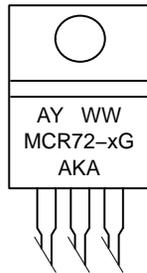


Figure 4. Gate Voltage

# MCR72-3, MCR72-6, MCR72-8

## MARKING DIAGRAMS

**TO-220AB  
CASE 221A-07**



**TO-220AB  
CASE 221A-09**



A = Assembly Location  
 Y = Year  
 WW = Work Week  
 MCR72-x = Device Code  
 x = 3, 6, 8, or 8T  
 G = Pb-Free Package  
 AKA = Diode Polarity

A = Assembly Location  
 Y = Year  
 WW = Work Week  
 MCR72-6T = Device Code  
 G = Pb-Free Package  
 AKA = Diode Polarity

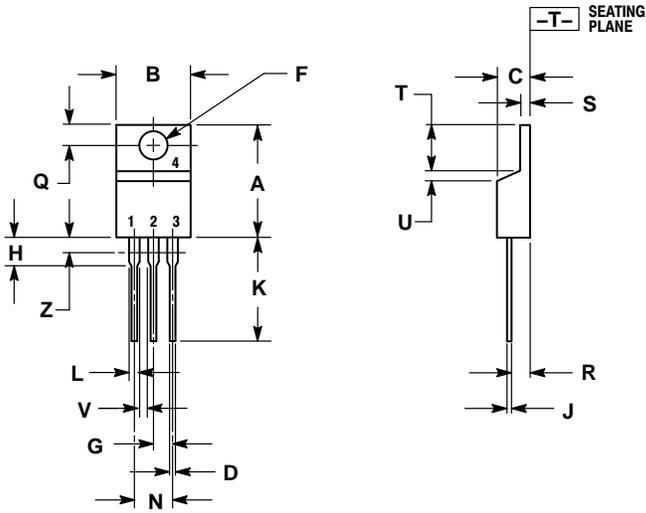
## ORDERING INFORMATION

Device	Package	Shipping
MCR72-3G	TO-220AB (Pb-Free)	500 Units / Box
MCR72-6G	TO-220AB (Pb-Free)	500 Units / Box
MCR72-6TG	TO-220AB (Pb-Free)	50 Units / Rail
MCR72-8G	TO-220AB (Pb-Free)	500 Units / Box
MCR72-8TG	TO-220AB (Pb-Free)	50 Units / Rail

# MCR72-3, MCR72-6, MCR72-8

## PACKAGE DIMENSIONS

TO-220  
CASE 221A-07  
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.022	0.36	0.55
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

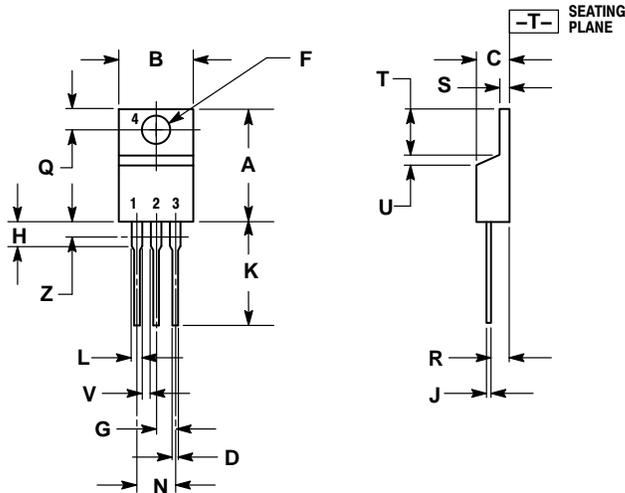
STYLE 3:

- PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

# MCR72-3, MCR72-6, MCR72-8

## PACKAGE DIMENSIONS

TO-220  
CASE 221A-09  
ISSUE AH



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
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U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 3:

- PIN 1: CATHODE  
2. ANODE  
3. GATE  
4. ANODE

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