Keywords: watchdog circuit, switching converters, linear regulators

APPLICATION NOTE 3626

Adding a Watchdog to a Dual-Output Power Supply

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Abstract: This circuit converts an unused linear-regulator output to a watchdog timer for monitoring software execution.

The design of low-cost consumer products like set-top boxes and DSL modems often requires a main logic supply in addition to the core voltage, so the power supply often provides multiple output voltages. Such multiple-output ICs include the MAX1864 (single-buck switching regulator and two linear outputs), and the MAX1865 (single-buck switching regulator and four linear outputs). If you incorporate either of these ICs in your system and one of the linear outputs remains unused, you can further integrate the design by converting that linear-regulator capability into a watchdog timer (**Figure 1**).
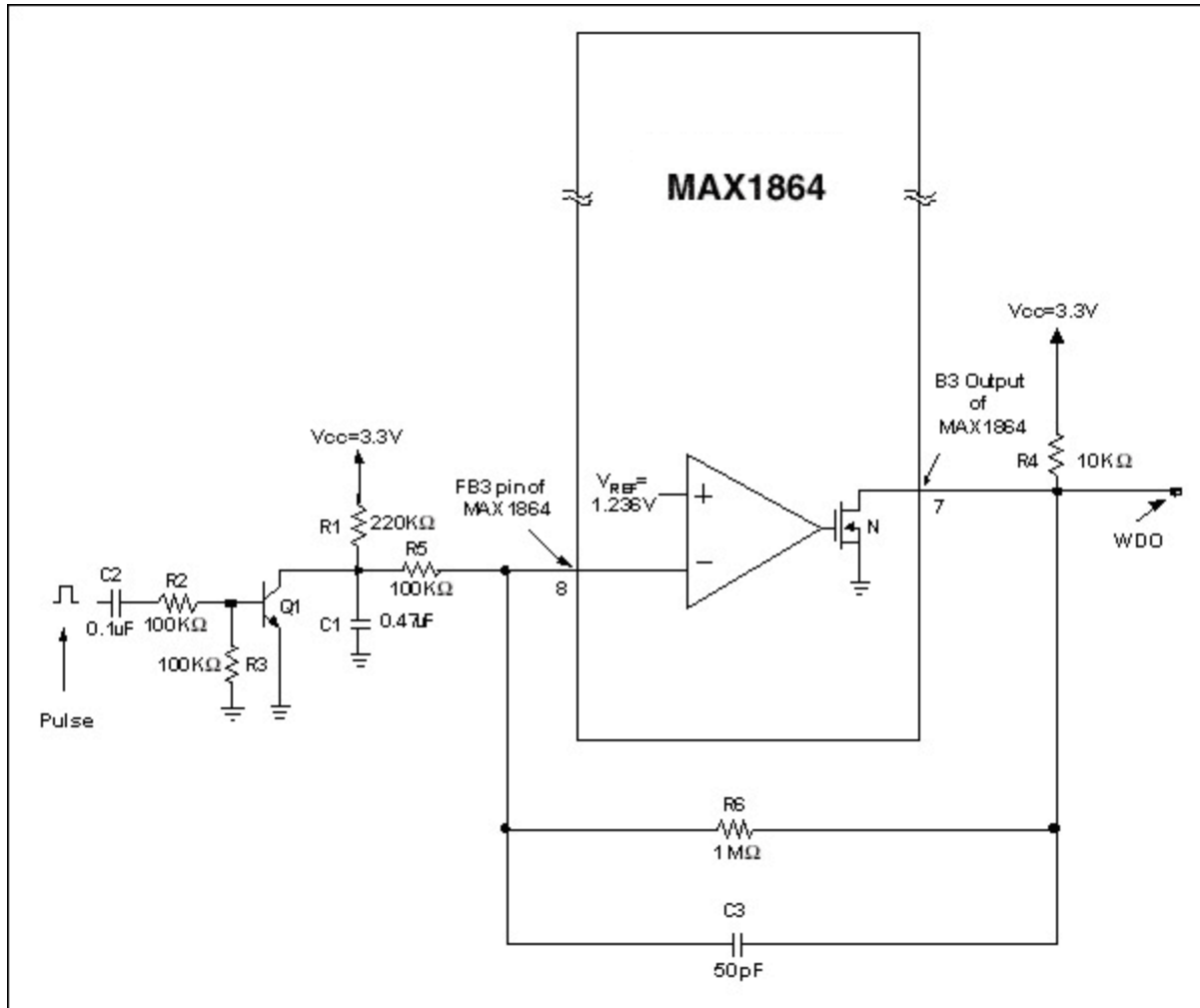
Figure 1. The external components shown convert this unused linear-regulator output (otherwise idle) into a watchdog timer.

R1 and C1 produce an RC time constant equal to the desired timeout period. Transistor Q1 and the passive components in its base circuit provide the watchdog's one-shot and reset functions. First, choose a watchdog timeout period and select R1 and C1. R1 can be calculated as

$$R1 = timeout/(C_{1ln}(1.236/V_{OUT}))$$

If we let the timeout interval equal 100msec, C1 = 0.47µF, and V_{OUT} = 3.3V, then R1 = 217kΩ. The nearest standard value is 220kΩ.

Q1 is a low-cost NPN bipolar transistor needed to discharge C1 during the timer's reset function. R2 and R3 maintain C2 in a zero-charge state, hold off Q1, and limit current into the base of Q1. R2-R3 values are not critical, so they are set at 100kΩ.

A value of 0.1mF is selected for C2, which provides AC coupling (highly recommended) between the microcontroller and watchdog circuitry. Coupling ensures generation of the expected watchdog timeout when a locked-up microcontroller forces its output either low or high. (Without AC coupling, the timer might be disabled.) R5, R6, and C3 form a hysteresis network that prevents oscillation during the

comparator transition.

A microcontroller must reset the timer before capacitor C1 charges to the 1.236V threshold of the MAX1864/MAX1865. The control signal should generally be logic low. Then assert a positive-going control pulse that returns to logic low in the inactive state. The pulse duration depends on the component values selected, but it only needs to ensure that C1 is discharged when the pulse terminates. To avoid the possibility of false timeouts with a 100msec watchdog interval, the reset pulses should occur at maximum intervals of approximately 30msec.

A different version of this application note appeared in the July 2005 issue of *Power Electronics Technology*

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