1.0 GHz to 1.9 GHz Tunable Band-Pass Filter

Data Sheet **HMC890ALP5E**

FEATURES

Amplitude settling time: 200 ns
Excellent wideband rejection: ≥30 dB
Single chip replacement for mechanically tuned designs
32-lead, 5 mm × 5 mm, RoHS compliant LFCSP package

APPLICATIONS

Test and measurement equipment
Military radar and electronic warfare/electronic countermeasures
Satellite communications and space
Industrial and medical equipment

FUNCTIONAL BLOCK DIAGRAM

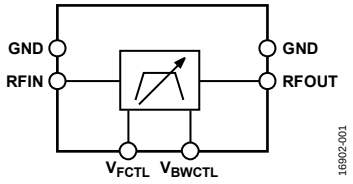

Figure 1.

GENERAL DESCRIPTION

The HMC890ALP5E is a monolithic microwave integrated circuit (MMIC), band-pass filter that features a user selectable pass-band frequency. The 3 dB filter bandwidth is approximately 10%. The ≥20 dB filter bandwidth is approximately 30%. The center frequency can vary between 1.0 GHz and 1.9 GHz by applying an analog tuning voltage between 0 V and 14 V.

This tunable filter can be used as a much smaller alternative to physically large switched filter banks and cavity tuned filters.

The HMC890ALP5E has excellent microphonics due to the monolithic design, and provides a dynamically adjustable solution in advanced communications applications.

Rev. 0 **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support **www.analog.com**

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REVISION HISTORY

8/2018—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_{FCTL} = V_{BWCTL}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY TUNING RANGE					
Center (f_{CENTER})	1.0		1.9	GHz	
BANDWIDTH					
3 dB		10		%	
3 dB Bandwidth Control (V_{BWCTL})		±3		%	
REJECTION					
Low-Side		0.87 × f_{CENTER}		GHz	≥20 dB
High-Side		1.17 × f_{CENTER}		GHz	≥20 dB
Reentry		4.30 × f_{CENTER}		GHz	≤30 dB
LOSS					
Insertion Loss		12		dB	
Return Loss		10		dB	
DYNAMIC PERFORMANCE					
Max Input Power for Linear Operation			10	dBm	
Input Third-Order Intercept (IP3)		35		dBm	Input power (P_{IN}) = 20 dBm per tone
Group Delay		4		ns	
Phase Sensitivity		2		Rad/V	
Amplitude Settling Time		200		ns	Time to settle to minimum insertion loss, within ≤0.5 dB of static insertion loss
Drift Rate		1.1		MHz/°C	
RESIDUAL PHASE NOISE					
At 1 MHz Offset		−155		dBc/Hz	
TUNING					
Voltages (V_{FCTL}, V_{BWCTL})	0		14	V	Each pin can be driven independently
Currents (I_{FCTL}, I_{BWCTL})			±1	µA	Rated current for each pin

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Tuning	
Voltages (V_{FCTL}, V_{BWCTL})	−0.5 V to +15 V
Currents (I_{FCTL}, I_{BWCTL})	±1 mA
Radio Frequency (RF) Input Power	27 dBm
Temperature	
Operating Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction for 1 Million Mean Time to Failure (MTTF)	175°C
Nominal Junction (Pad Temperature (T_{PAD}) = 85°C, P_{IN} = 10 dBm)	90°C
Electrostatic Discharge (ESD)	
Human Body Model (HBM)	1500 V
Field Induced Charge Device Model (FICDM)	1250 V
Moisture Sensitivity Level (MSL) Rating	MSL3

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

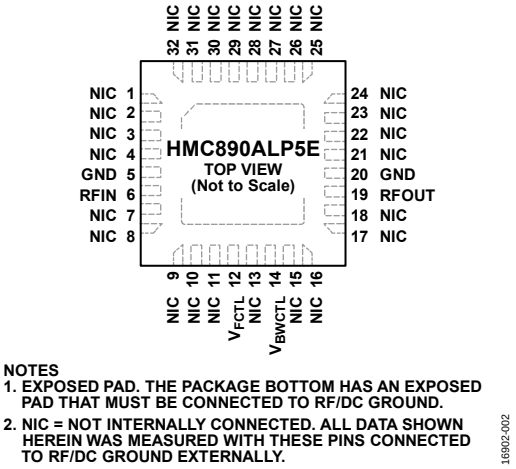


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4, 7 to 11, 13, 15 to 18, 21 to 32	NIC	Not Internally Connected. All data shown herein was measured with these pins connected to RF/dc ground externally.
5, 20	GND	Ground. These pins and the exposed pad must be connected to RF/dc ground.
6	RFIN	Radio Frequency Input. This pin is dc-coupled and is matched to 50 Ω. Do not apply external voltage to this pin.
12	V_{FCTL}	Center Frequency Control Voltage.
14	V_{BWCTL}	Bandwidth Control Voltage.
19	RFOUT	Radio Frequency Output. This pin is dc-coupled and is matched to 50 Ω. Do not apply external voltage to this pin.
	EPAD	Exposed Pad. The package bottom has an exposed pad that must be connected to RF/dc ground.

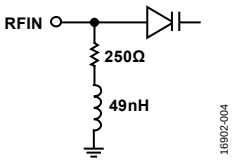


Figure 3. RFIN Interface Schematic

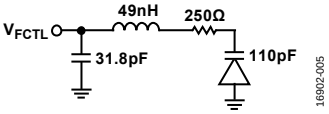


Figure 4. V_{FCTL} Interface Schematic

Figure 5. GND Interface Schematic

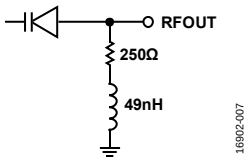


Figure 6. RFOUT Interface Schematic

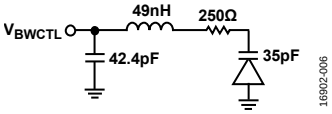


Figure 7. V_{BWCTL} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

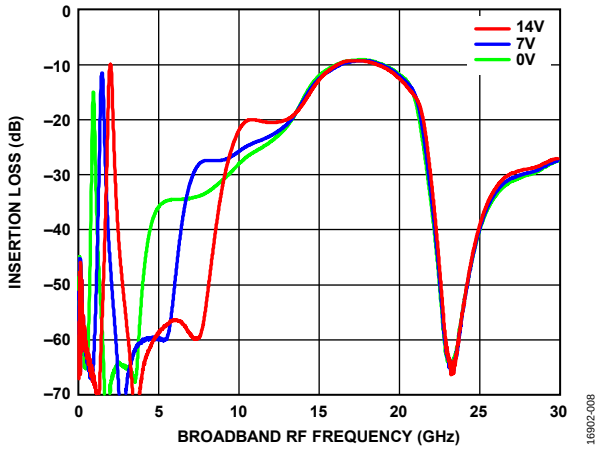


Figure 8. Insertion Loss vs. Broadband RF Frequency at Various Voltages ($V_{FCTL} = V_{BWCTL}$)

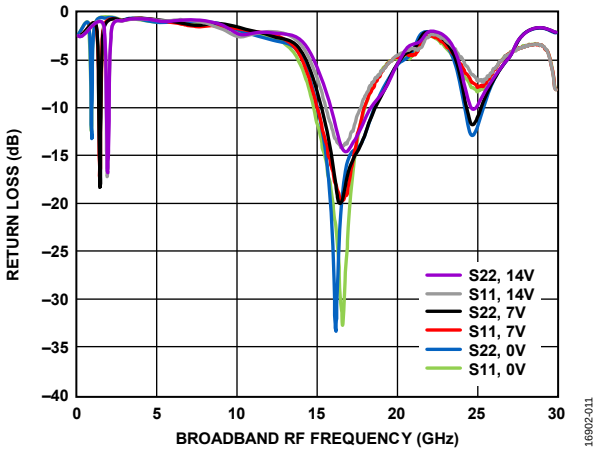


Figure 11. Return Loss vs. Broadband RF Frequency at Various Voltages ($V_{FCTL} = V_{BWCTL}$)

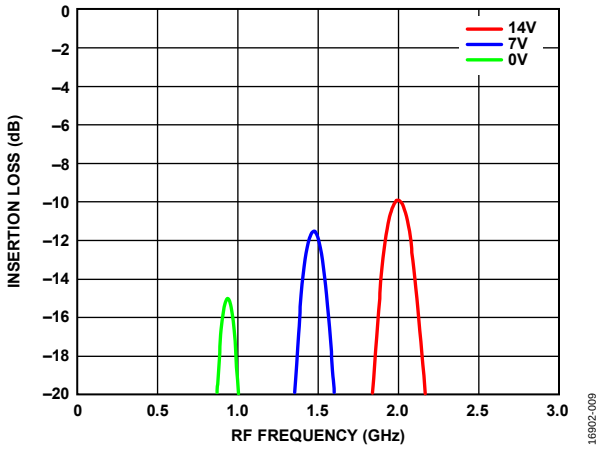


Figure 9. Insertion Loss vs. RF Frequency at Various Voltages ($V_{FCTL} = V_{BWCTL}$)

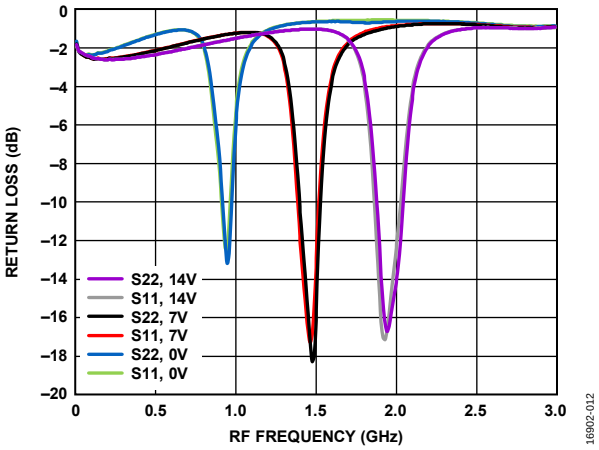


Figure 12. Return Loss vs. RF Frequency at Various Voltages ($V_{FCTL} = V_{BWCTL}$)

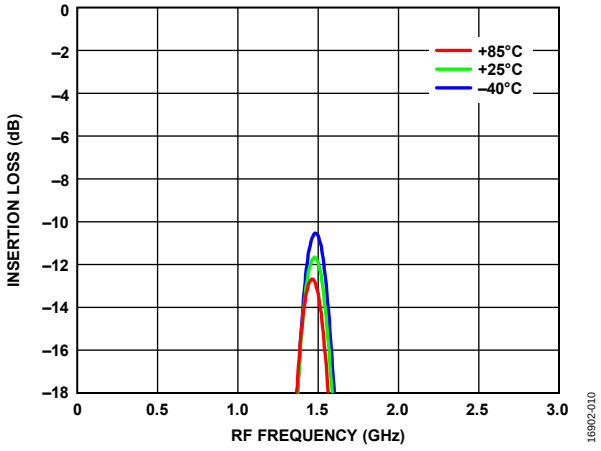


Figure 10. Insertion Loss vs. RF Frequency at Various Temperatures, $V_{FCTL} = V_{BWCTL} = 7$ V

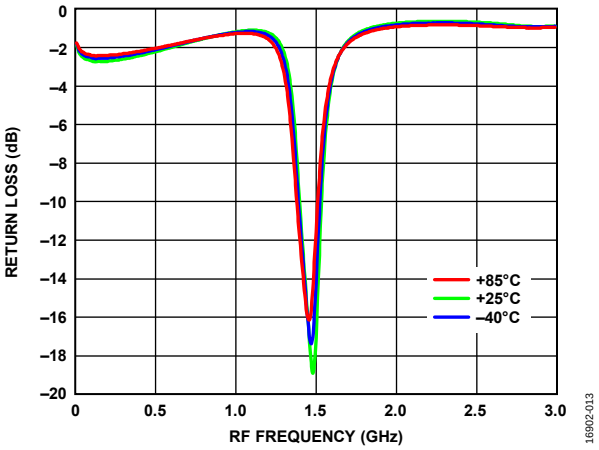


Figure 13. Return Loss vs. RF Frequency at Various Temperatures, $V_{FCTL} = V_{BWCTL} = 7$ V

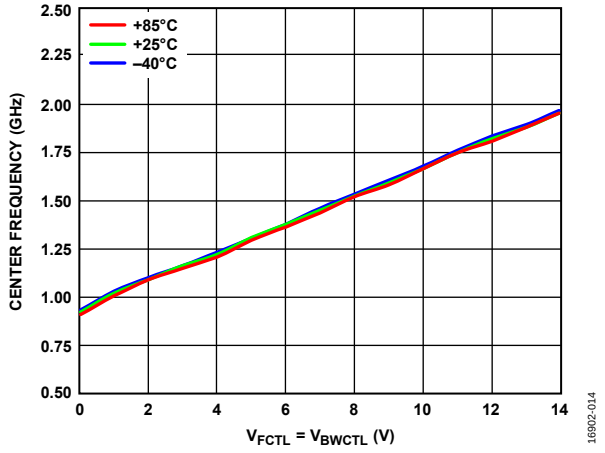


Figure 14. Center Frequency vs. $V_{FCTL} = V_{BWCTL}$ at Various Temperatures

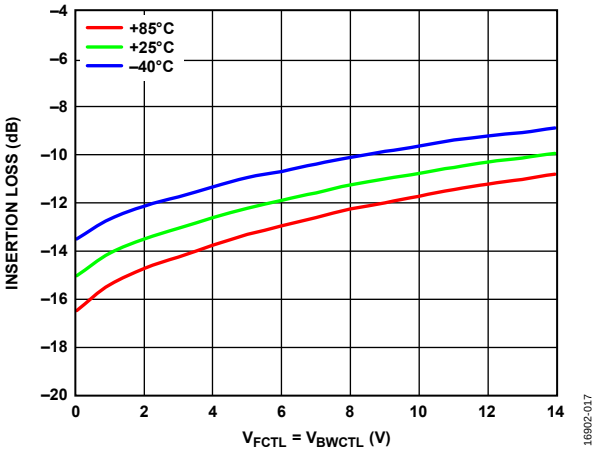


Figure 17. Insertion Loss vs. $V_{FCTL} = V_{BWCTL}$ at Various Temperatures

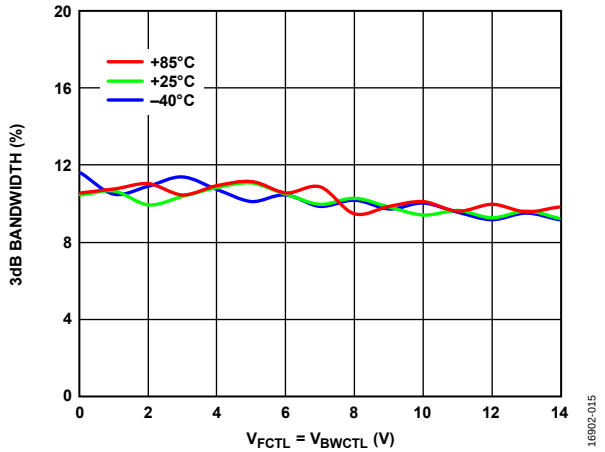


Figure 15. 3 dB Bandwidth vs. $V_{FCTL} = V_{BWCTL}$ at Various Temperatures

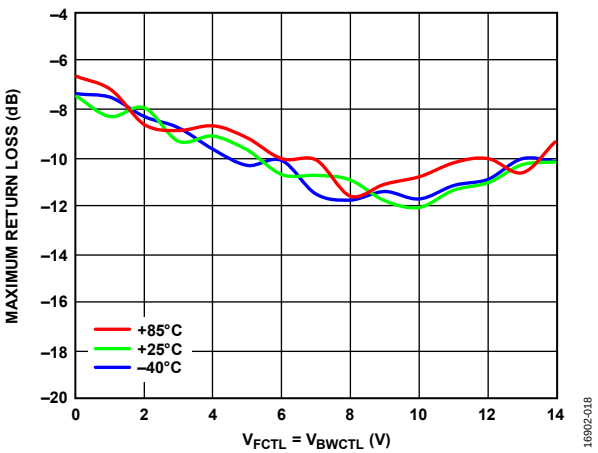


Figure 18. Maximum Return Loss in a 2 dB Bandwidth vs. $V_{FCTL} = V_{BWCTL}$ at Various Temperatures

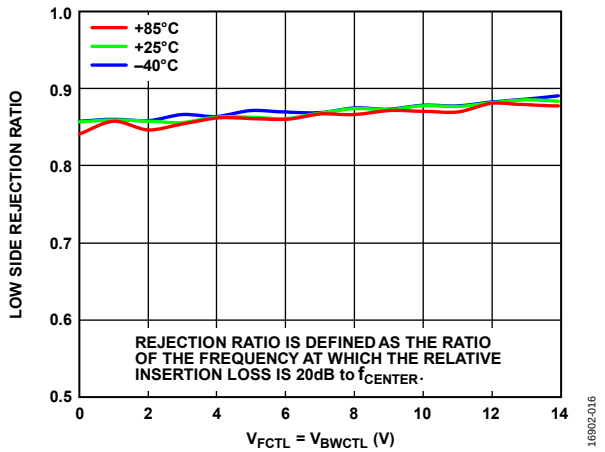


Figure 16. Low-Side Rejection Ratio vs. $V_{FCTL} = V_{BWCTL}$ at Various Temperatures

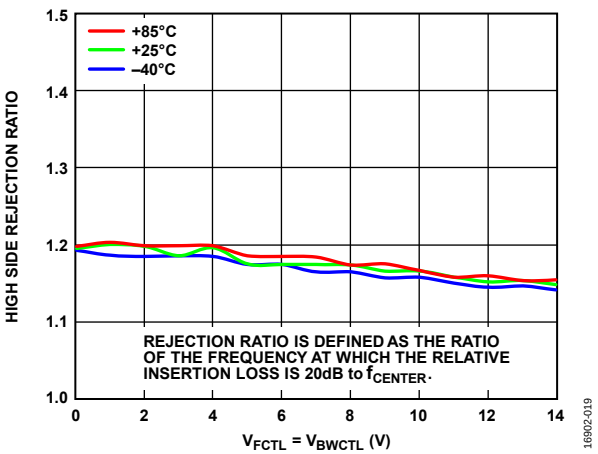


Figure 19. High-Side Rejection Ratio vs. $V_{FCTL} = V_{BWCTL}$ at Various Temperatures

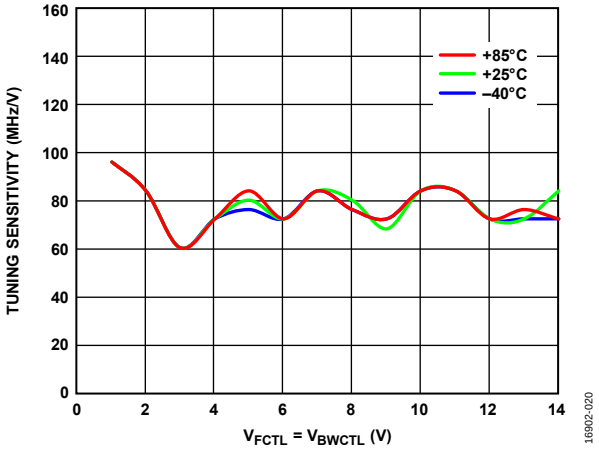


Figure 20. Tuning Sensitivity vs. $V_{FCTL} = V_{BWCTL}$ at Various Temperatures

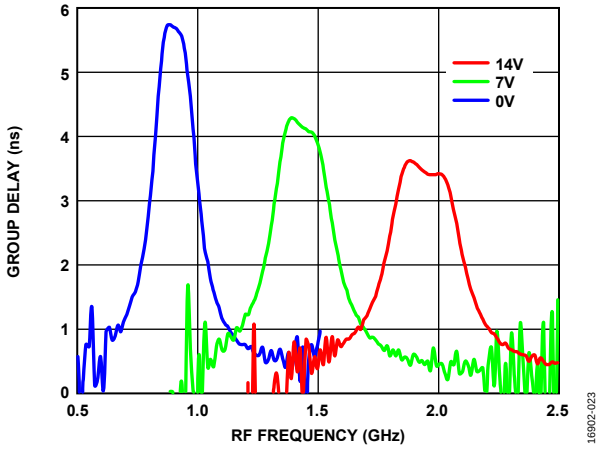


Figure 23. Group Delay vs. RF Frequency at Various $V_{FCTL} = V_{BWCTL}$ Voltages

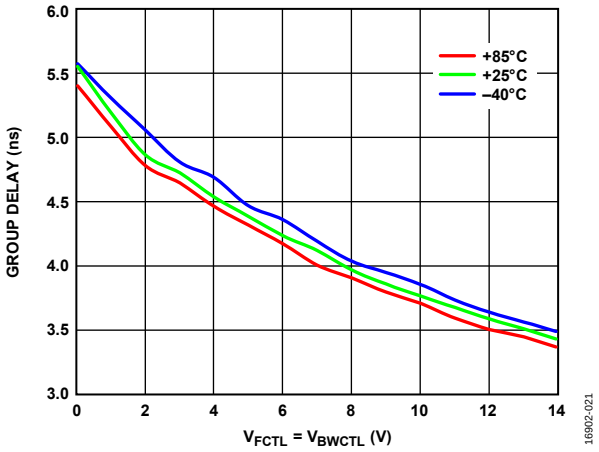


Figure 21. Group Delay vs. $V_{FCTL} = V_{BWCTL}$ at Various Temperatures

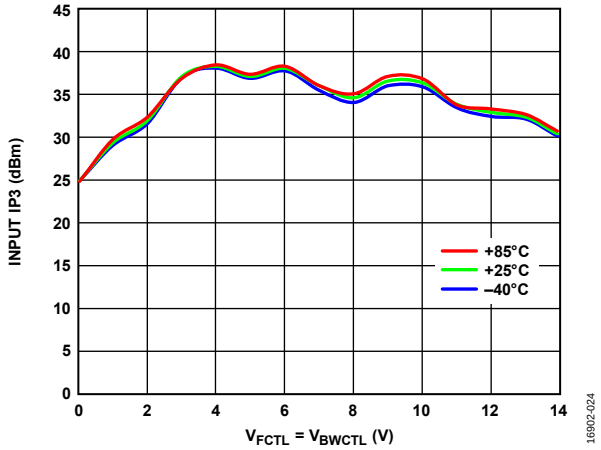


Figure 24. Input IP3 vs. $V_{FCTL} = V_{BWCTL}$ at Various Temperatures, Input Power = 20 dBm

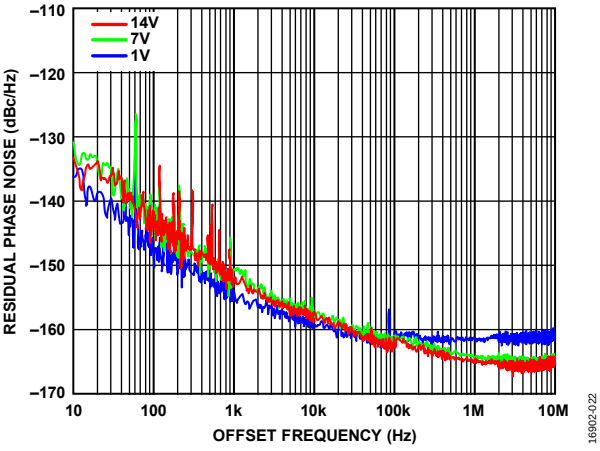


Figure 22. Residual Phase Noise vs. Offset Frequency at Various $V_{FCTL} = V_{BWCTL}$ Voltages

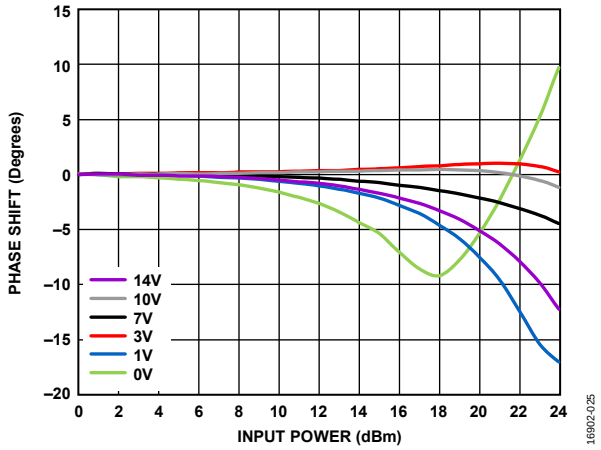


Figure 25. Phase Shift vs. Input Power at Various $V_{FCTL} = V_{BWCTL}$ Values

THEORY OF OPERATION

The HMC890ALP5E is a MMIC band-pass filter that features a user selectable pass-band frequency. Varying the applied analog tuning voltage between 0 V and 14 V at V_{FCTL} varies the center frequency between 1.0 GHz and 1.9 GHz. The bandwidth of the filter is adjustable by using the V_{BWCTL} control voltage, which can vary from 0 V to 14 V. It is the typical operation to tie the V_{FCTL} and V_{BWCTL} control voltages together

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

Figure 26 shows the typical application circuit for the HMC890ALP5E. The RFIN pin and RFOUT pin are dc-coupled and require external 100 pF series capacitors (C1 and C2).

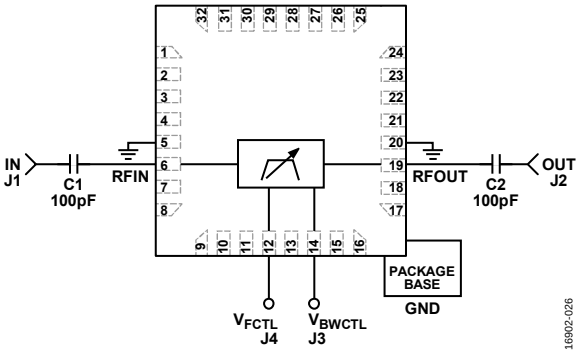


Figure 26. Typical Application Circuit

EVALUATION PRINTED CIRCUIT BOARD (PCB) INFORMATION

All RF traces are routed on Layer 1 (primary side), and all other layers are ground planes that provide a solid ground for RF transmission lines, as shown in Figure 27. The top dielectric material is Rogers 4350, offering low loss performance. The prepreg material in Layer 2 attaches the Isola 370HR with copper traces layers above and below together. Both the prepreg material and the Isola 370HR core layer are used to achieve the required board finish thickness.

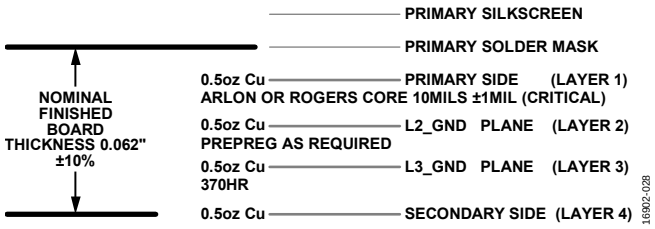


Figure 27. 4-Layer Stackup

The circuit board used in the application uses RF circuit design techniques. Signal lines must have 50 Ω impedance while the package ground leads and exposed pad must be connected directly to the ground plane (see Figure 28). Use a sufficient number of via holes to connect the top and bottom ground planes. The EV1HMC890ALP5 evaluation board shown in Figure 28 is available from Analog Devices, Inc., upon request.

Table 4. Bill of Materials

Item	Description
J1 to J2	PCB mount Subminiature Version A (SMA) RF connectors, SRI
J3 to J4	PCB mount SMA RF connectors, Johnson
U1	HMC890ALP5E
PCB[1]	08-049598[2] evaluation PCB

[1] Circuit board material: Arlon 25FR or Rogers 25FR.
[2] 08-049598 is the raw bare PCB identifier. Reference EV1HMC890ALP5 when ordering complete evaluation PCB.

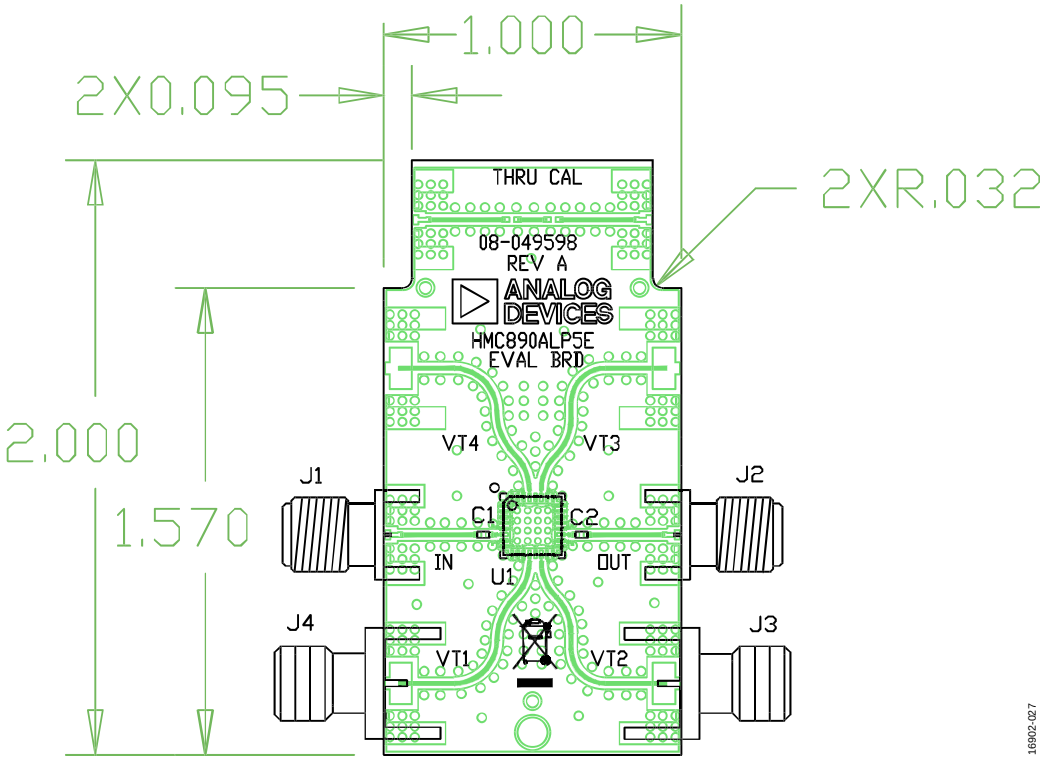
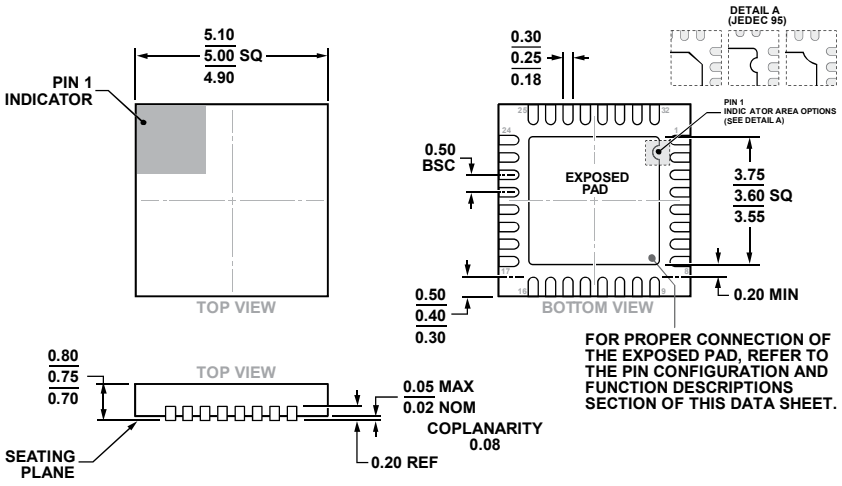


Figure 28. EV1HMC890ALP5 Evaluation Board, Dimensions Shown in Inches

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-5

Figure 29. 32-Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
HMC890ALP5E	−40°C to +85°C	32-Lead Frame Chip Scale Package [LFCSP]	CP-32-12
HMC890ALP5ETR	−40°C to +85°C	32-Lead Frame Chip Scale Package [LFCSP]	CP-32-12
EV1HMC890ALP5		Evaluation PCB	

[1] All models are RoHS compliant parts.