Six Degrees of Freedom Inertial Sensor

Data Sheet

ADIS16385

FEATURES

- Tri-axis digital gyroscope with digital range scaling
  - ±75°/sec, ±150°/sec, ±300°/sec settings
  - Orthogonal alignment: <0.05°
- In-run bias stability: 6°/hour (yaw), 21°/hour (pitch/roll)
- Tri-axis digital accelerometer: ±5 *g*
- Autonomous operation and data collection
  - No external configuration commands required
  - Start-up time: 210 ms
  - Sleep mode recovery time: 7 ms
- Factory-calibrated sensitivity, bias, and axial alignment
- Calibration temperature range: −40°C to +85°C
- Single serial peripheral interface, SPI-compatible
- Wide bandwidth: 330 Hz
- Embedded temperature sensor
- Programmable operation and control
  - Automatic and manual bias correction controls
  - Digital filters: Bartlett FIR, average/decimation
  - Digital I/O: data-ready, alarm indicator, general-purpose
  - Alarms for condition monitoring
  - Sleep mode for power management
  - DAC output voltage
  - Enable external sample clock input: up to 1.2 kHz
- Single-supply operation: 4.85 V to 5.15 V
- 2000 *g* shock survivability
- Operating temperature range: −40°C to +105°C

APPLICATIONS

- Platform stabilization and control
- Navigation
- Robotics

FUNCTIONAL BLOCK DIAGRAM

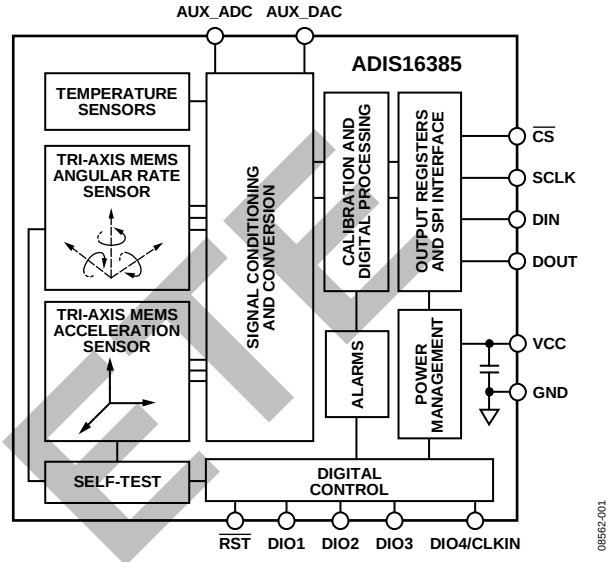

Figure 1.

GENERAL DESCRIPTION

The ADIS16385 *i*Sensor® device is a complete inertial system that includes a tri-axis gyroscope and tri-axis accelerometer. Each sensor in the ADIS16385 combines industry-leading *i*MEMS® technology with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, alignment, and linear acceleration (gyro bias). As a result, each sensor has its own dynamic compensation formulas that provide accurate sensor measurements. The yaw-axis gyroscope offers a 4× improvement in noise and in-run bias stability for applications that have greater requirements on one axis.

The ADIS16385 provides a simple, cost-effective method for integrating accurate, multiaxis inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. The SPI and register structure provide a simple interface for data collection and configuration control.

The ADIS16385 has a compatible pinout for systems that currently use ADIS1635x, ADIS1636x, and ADIS1640x IMU products. It comes in a module that is approximately 36 mm × 47 mm × 39 mm and has a standard connector interface.

Rev. B

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SPECIFICATIONS

T_A = 25°C, VCC = 5.0 V, angular rate = 0°/sec, dynamic range = ±300°/sec ± 1 *g*, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range		±300	±350		°/sec
Initial Sensitivity	Dynamic range = ±300°/sec	0.012375	0.0125	0.12625	°/sec/LSB
	Dynamic range = ±150°/sec		0.00625		°/sec/LSB
	Dynamic range = ±75°/sec		0.003125		°/sec/LSB
Sensitivity Temperature Coefficient	−40°C ≤ T_A ≤ +85°C		±40		ppm/°C
Misalignment Error	Axis to axis		±0.05		Degrees
	Axis-to-frame (package)		±0.5		Degrees
Nonlinearity	Best fit straight line		±0.1		% of FS
Initial Bias Error	±1 σ		±3		°/sec
In-Run Bias Stability	1 σ, +25°C, z-axis		0.0017		°/sec
	1 σ, +25°C, x-axis, y-axis		0.0057		°/sec
Angular Random Walk	Z-axis, 1 σ, +25°C		0.75		°/√hr
	X-axis, y-axis, 1 σ, +25°C		1.9		°/√hr
Bias Temperature Coefficient	Z-axis, −40°C ≤ T_A ≤ +85°C		0.001		°/sec/°C
	X-axis, y-axis, −40°C ≤ T_A ≤ +85°C		0.004		°/sec/°C
Linear Acceleration Effect on Bias	Z-axis, 1 σ (MSC_CTRL[7] = 1)		±0.03		°/sec/*g*
	X-axis, y-axis, 1 σ (MSC_CTRL[7] = 1)		±0.05		°/sec/*g*
Bias Voltage Sensitivity	Z-axis, VCC = 4.85 V to 5.15 V		±0.02		°/sec/V
	X-axis, y-axis, VCC = 4.85 V to 5.15 V		±0.1		°/sec/V
Output Noise	Z-axis, ±300°/sec range, no filtering		0.27		°/sec rms
	X-axis, y-axis, ±300°/sec range, no filtering		0.75		°/sec rms
Rate Noise Density	Z-axis, f = 25 Hz, ±300°/sec range		0.0122		°/sec/√Hz rms
	X-axis, y-axis, f = 25 Hz, ±300°/sec range		0.04		°/sec/√Hz rms
3 dB Bandwidth			330		Hz
Sensor Resonant Frequency			14.5		kHz
Self-Test Change in Output Response	±300°/sec range setting	±2784		±9796	LSB
ACCELEROMETERS	Each axis				
Dynamic Range		±5			*g*
Initial Sensitivity		0.2475	0.25	0.2525	m*g*/LSB
Sensitivity Temperature Coefficient	−40°C ≤ T_A ≤ +85°C		±40		ppm/°C
Misalignment Error	Axis-to-axis		±0.1		Degrees
	Axis-to-frame (package)		±0.5		Degrees
Nonlinearity	Best fit straight line		±0.1		% of FS
Initial Bias Error	±1 σ		±10		m*g*
In-Run Bias Stability	1 σ		50		µ*g*
Velocity Random Walk	1 σ		0.09		m/sec/√hr
Bias Temperature Coefficient	−40°C ≤ T_A ≤ +85°C		±0.023		m*g*/°C
Bias Voltage Sensitivity	VCC = 4.85 V to 5.15 V		2		m*g*/V
Output Noise	No filtering		3.3		m*g* rms
Noise Density	No filtering		180		µ*g*/√Hz rms
3 dB Bandwidth			330		Hz
Sensor Resonant Frequency			5.5		kHz
Self-Test Change in Output Response	X-axis and y-axis	560		2280	LSB
TEMPERATURE SENSOR					
Scale Factor	Output = 0x0000 at 25°C (±5°C)		0.0678		°C/LSB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC INPUT					
Resolution			12		Bits
Integral Nonlinearity			±2		LSB
Differential Nonlinearity			±1		LSB
Offset Error			±4		LSB
Gain Error			±2		LSB
Input Range		0		3.3	V
Input Capacitance	During acquisition		20		pF
DAC OUTPUT	5 kΩ/100 pF to GND				
Resolution			12		Bits
Relative Accuracy	101 LSB ≤ input code ≤ 4095 LSB		±4		LSB
Differential Nonlinearity			±1		LSB
Offset Error			±5		mV
Gain Error			±0.5		%
Output Range		0		3.3	V
Output Impedance			2		Ω
Output Settling Time			10		µs
LOGIC INPUTS[1]					
Input High Voltage, V_{IH}		2.0			V
Input Low Voltage, V_{IL}				0.8	V
	$\overline{CS}$ signal to wake up from sleep mode			0.55	V
$\overline{CS}$ Wake-Up Pulse Width		20			µs
Logic 1 Input Current, I_{IH}	V_{IH} = 3.3 V		±0.2	±10	µA
Logic 0 Input Current, I_{IL}	V_{IL} = 0 V				
All Pins Except $\overline{RST}$			40	60	µA
$\overline{RST}$ Pin			1		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS[1]					
Output High Voltage, V_{OH}	I_{SOURCE} = 1.6 mA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 1.6 mA			0.4	V
FLASH MEMORY	Endurance[2]	10,000			Cycles
Data Retention[3]	T_J = 85°C	20			Years
FUNCTIONAL TIMES[4]	Time until data is available				
Power-On Start-Up Time			210		ms
Reset Recovery Time			90		ms
Sleep Mode Recovery Time			7		ms
Flash Memory Test Time			30		ms
Automatic Self-Test Time	SMPL_PRD = 0x0001		52		ms
CONVERSION RATE	SMPL_PRD = 0x0001		1024		SPS
Clock Accuracy				±3	%
Sync Input Clock[5]		0.8		1.2	kHz
POWER SUPPLY	Operating voltage range, VCC	4.85	5.0	5.15	V
Power Supply Current			132		mA
	Sleep mode		1.4		mA

[1] The digital I/O signals are driven by an internal 3.3 V supply, and the inputs are 5 V tolerant.
[2] Endurance is qualified as per JEDEC Standard 22, Method A117, and measured at −40°C, +25°C, +85°C, and +125°C.
[3] The data retention lifetime equivalent is at a junction temperature (T_J) of 85°C as per JEDEC Standard 22, Method A117. Data retention lifetime decreases with junction temperature.
[4] These times do not include thermal settling and internal filter response times (330 Hz bandwidth), which may affect overall accuracy.
[5] The sync input clock functions below the specified minimum value, at reduced performance levels.

TIMING SPECIFICATIONS

T_A = 25°C, VCC = 5 V, unless otherwise noted.

Table 2.

Parameter	Description	Normal Mode			Burst Read			Unit
		Min[1]	Typ	Max	Min[1]	Typ	Max	
f_{SCLK}	Serial clock	0.01		2.0	0.01		1.0	MHz
t_{STALL}	Stall period between data	9			$1/f_{SCLK}$			µs
$t_{READRATE}$	Read rate	40						µs
$t_{\overline{CS}}$	Chip select to clock edge	48.8			48.8			ns
t_{DAV}	DOUT valid after SCLK edge			100			100	ns
t_{DSU}	DIN setup time before SCLK rising edge	24.4			24.4			ns
t_{DHD}	DIN hold time after SCLK rising edge	48.8			48.8			ns
t_{SCLKR}, t_{SCLKF}	SCLK rise/fall times		5	12.5		5	12.5	ns
t_{DR}, t_{DF}	DOUT rise/fall times		5	12.5		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	5			5			ns
t_1	Input sync positive pulse width	5			5			µs
t_x	Input sync low time	100			100			µs
t_2	Input sync to data-ready output		600			600		µs
t_3	Input sync period	833			833			µs

[1] Guaranteed by design and characterization, but not tested in production.

Timing Diagrams

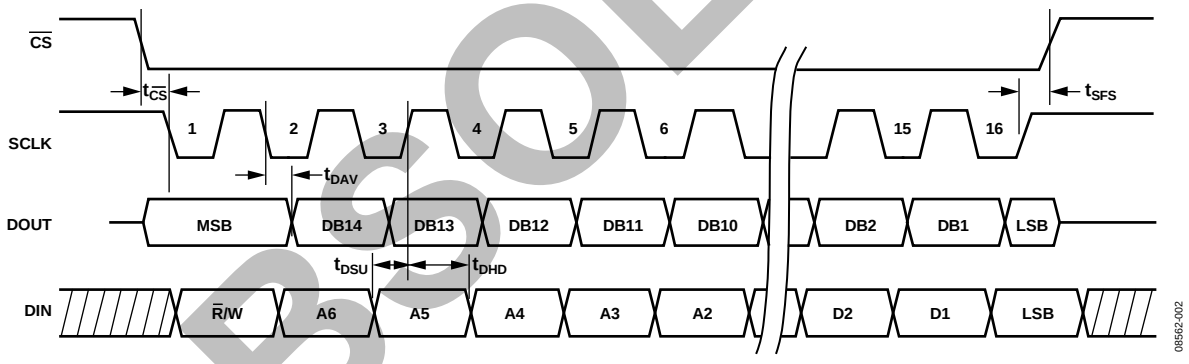


Figure 2. SPI Timing and Sequence

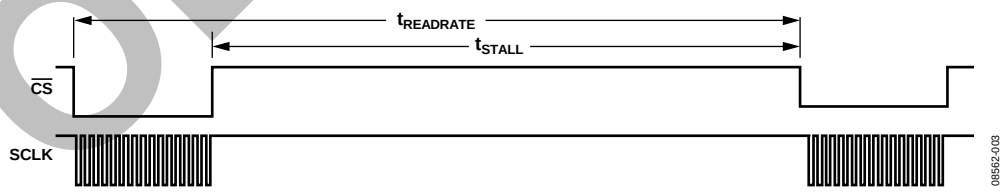


Figure 3. Stall Time and Data Rate

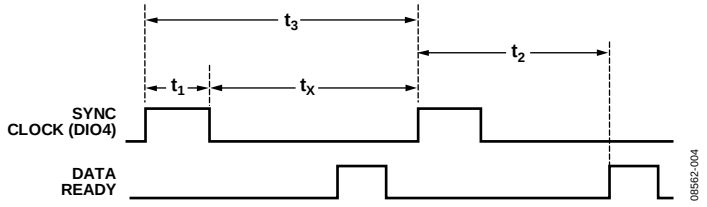


Figure 4. Input Clock Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	2000 *g*
Any Axis, Powered	2000 *g*
VCC to GND	−0.3 V to +7.0 V
Digital Input Voltage to GND	−0.3 V to +5.3 V
Digital Output Voltage to GND	−0.3 V to VCC + 0.3 V
Analog Input to GND	−0.3 V to +3.6 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +125°C[1, 2]

[1] Extended exposure to temperatures outside the specified temperature range of −40°C to +105°C can adversely affect the accuracy of the factory calibration. For best accuracy, store the parts within the specified operating range of −40°C to +105°C.
[2] Although the device is capable of withstanding short-term exposure to 150°C, long-term exposure threatens internal mechanical integrity.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Weight
24-Lead Module (ML-24-5)	39.8°C/W	14.2°C/W	59 grams

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

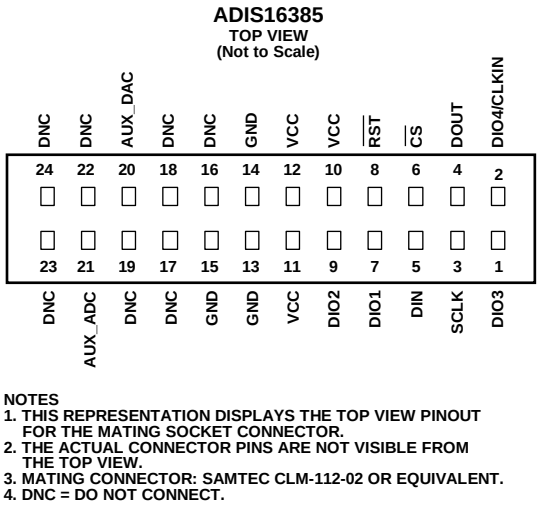


Figure 5. Pin Configuration

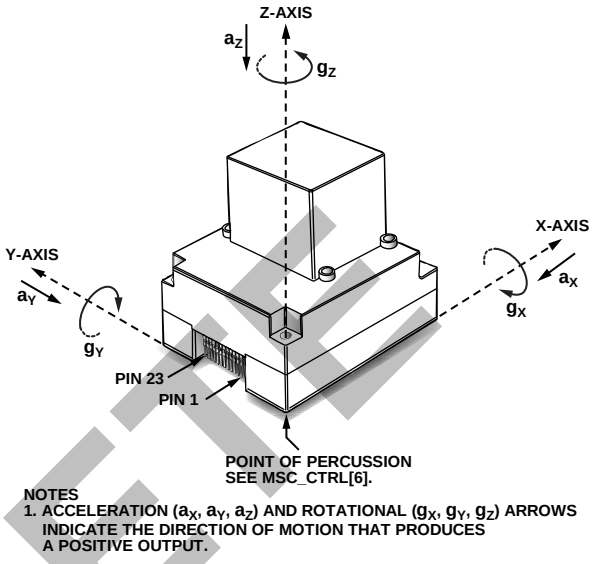


Figure 6. Axial Orientation

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	DIO3	I/O	Configurable Digital Input/Output.
2	DIO4/CLKIN	I/O	Configurable Digital Input/Output or Sync Clock Input.
3	SCLK	I	SPI Serial Clock.
4	DOUT	O	SPI Data Output. Clocks output on SCLK falling edge.
5	DIN	I	SPI Data Input. Clocks input on SCLK rising edge.
6	$\overline{CS}$	I	SPI Chip Select.
7, 9	DIO1, DIO2	I/O	Configurable Digital Input/Output.
8	$\overline{RST}$	I	Reset.
10, 11, 12	VCC	S	Power Supply.
13, 14, 15	GND	S	Power Ground.
16, 17, 18, 19, 22, 23, 24	DNC	N/A	Do Not Connect.
20	AUX_DAC	O	Auxiliary, 12-Bit DAC Output.
21	AUX_ADC	I	Auxiliary, 12-Bit ADC Input.

[1] I/O is input/output, I is input, O is output, S is supply, and N/A is not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

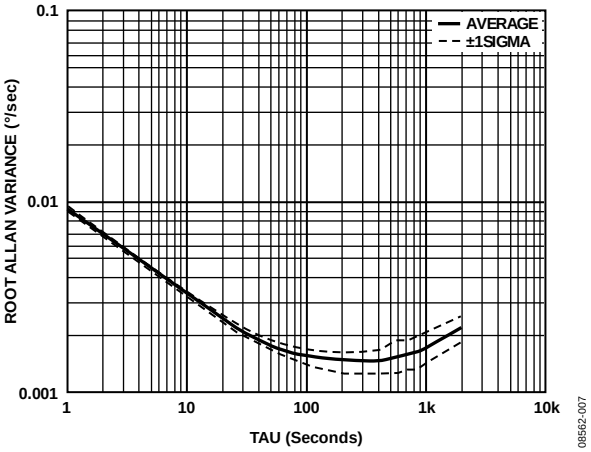


Figure 7. Gyroscope Allan Variance, Z-Axis

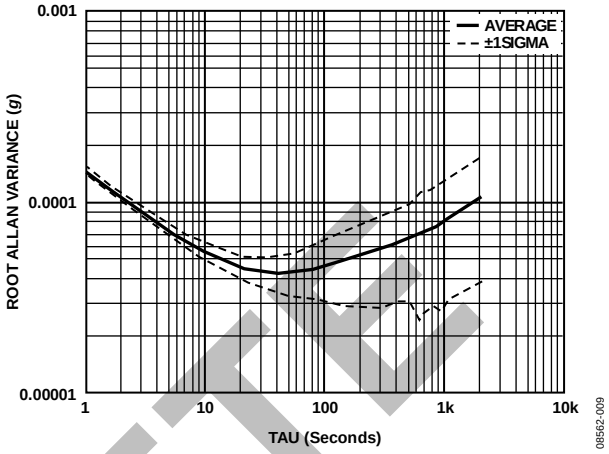


Figure 9. Accelerometer Allan Variance

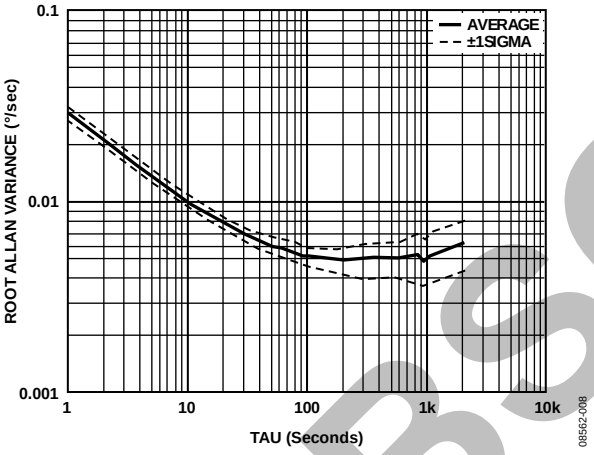


Figure 8. Gyroscope Allan Variance, X-Axis/Y-Axis

BASIC OPERATION

The ADIS16385 is an autonomous system that requires no user initialization. When it has a valid power supply, it initializes itself and starts sampling, processing, and loading sensor data into the output registers at a sample rate of 1024 SPS. DIO1 pulses high after each sample cycle concludes. The SPI interface enables simple integration with many embedded processor platforms, as shown in Figure 10 (electrical connection) and Table 6 (pin descriptions).

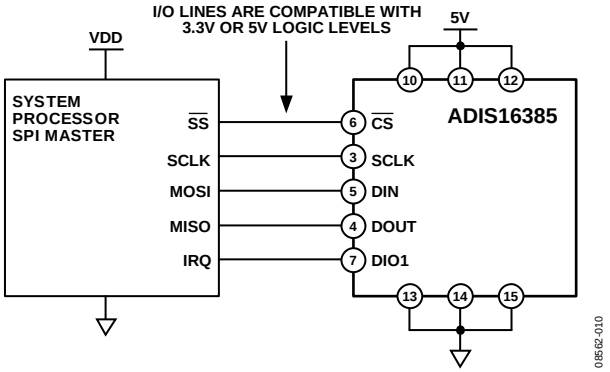


Figure 10. Electrical Connection Diagram

Table 6. Generic Master Processor Pin Names and Functions

Pin Name	Function
$\overline{SS}$	Slave select
SCLK	Serial clock
MOSI	Master output, slave input
MISO	Master input, slave output
IRQ	Interrupt request

The ADIS16385 SPI interface supports full-duplex serial communication (simultaneous transmit and receive) and uses the bit sequence shown in Figure 14. Table 7 provides a list of the most common settings that require attention to initialize a processor's serial port for the ADIS16385 SPI interface.

Table 7. Generic Master Processor SPI Settings

Processor Setting	Description
Master	The ADIS16385 operates as a slave
SCLK Rate ≤ 2 MHz[1]	Maximum serial clock rate
SPI Mode 3	CPOL = 1 (polarity), CPHA = 1 (phase)
MSB First Mode	Bit sequence
16-Bit Mode	Shift register/data length

[1] For burst read, SCLK rate ≤ 1 MHz.

READING SENSOR DATA

The ADIS16385 provides two different options for acquiring sensor data: single register and burst register. A single register read requires two 16-bit SPI cycles. The first cycle requests the contents of a register using the bit assignments in Figure 14. Bit DC7 to Bit DC0 are don't care for a read, and then the output register contents follow on DOUT during the second sequence. Figure 11 includes three single register reads in succession. In this example, the process starts with DIN = 0x0400 to request the contents of XGYRO_OUT, then follows with 0x0600 to request YGYRO_OUT and 0x0800 to request ZGYRO_OUT. Full-duplex operation enables processors to use the same 16-bit SPI cycle to read data from DOUT while requesting the next set of data on DIN. Figure 12 provides an example of the four SPI signals when reading XGYRO_OUT in a repeating pattern.

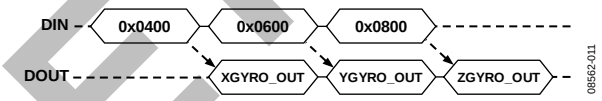


Figure 11. SPI Read Example

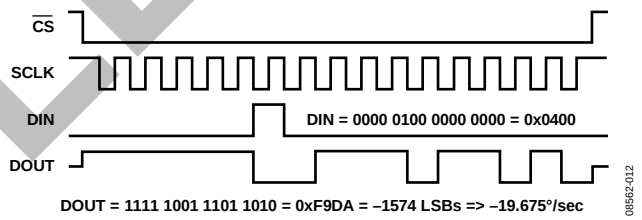


Figure 12. Example SPI Read, Second 16-Bit Sequence

Burst Read Function

The burst read function enables the user to read all output registers using one command on the DIN line and shortens the stall time between each 16-bit segment to one SCLK cycle (see Table 2). Figure 13 provides the burst read sequence of data on each SPI signal. The sequence starts with writing 0x3E00 to DIN, followed by each output register clocking out on DOUT, in the order in which they appear in Table 8.

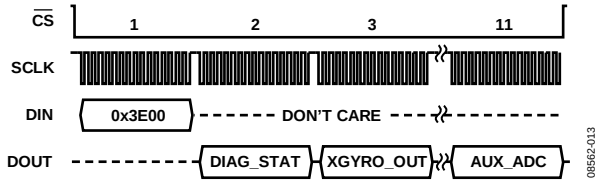
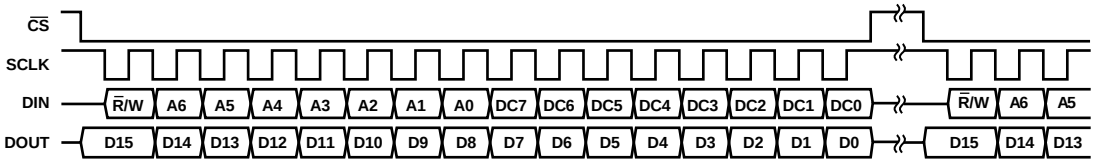


Figure 13. Burst Read Sequence



NOTES
1. THE DOUT BIT PATTERN REFLECTS THE ENTIRE CONTENTS OF THE REGISTER IDENTIFIED BY [A6:A0] IN THE PREVIOUS 16-BIT DIN SEQUENCE WHEN $\overline{R}/W$ = 0.
2. IF $\overline{R}/W$ = 1 DURING THE PREVIOUS SEQUENCE, DOUT IS NOT DEFINED.

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Figure 14. SPI Communication Bit Sequence

OUTPUT DATA REGISTERS

The output registers in Table 8 provide the most recent sensor data produced by the ADIS16385. All of the inertial sensor outputs use a 16-bit twos complement, data format. Figure 6 provides arrows to describe the direction of motion that produces a positive output in each inertial sensor's output data register.

Table 8. Output Data Register Formats

Register	Address	Measurement	Format
XGYRO_OUT[1]	0x04	Gyroscope, x-axis	Table 9
YGYRO_OUT[1]	0x06	Gyroscope, y-axis	Table 9
ZGYRO_OUT[1]	0x08	Gyroscope, z-axis	Table 9
XACCL_OUT	0x0A	Accelerometer, x-axis	Table 10
YACCL_OUT	0x0C	Accelerometer, y-axis	Table 10
ZACCL_OUT	0x0E	Accelerometer, z-axis	Table 10
TEMP_OUT[2]	0x10	Internal temperature	Table 11
AUX_ADC	0x12	Auxiliary ADC	Table 12

[1] Assumes that the scaling is set to ±300°/sec. This factor scales with the range.
[2] This is most useful for monitoring relative changes in the temperature.

Table 9. Rotation Rate, Twos Complement Format

Rotation Rate	Decimal	Hex	Binary
+300°/sec	+24000	0x5DC0	0101 1101 1100 0000
+0.025°/sec	+2	0x0002	0000 0000 0000 0010
+0.0125°/sec	+1	0x0001	0000 0000 0000 0001
0°/sec	0	0x0000	0000 0000 0000 0000
−0.0125°/sec	−1	0xFFFF	1111 1111 1111 1111
−0.025°/sec	−2	0xFFFE	1111 1111 1111 1110
−300°/sec	−24000	0xA240	1010 0010 0100 0000

Table 10. Acceleration, Twos Complement Format

Acceleration	Decimal	Hex	Binary
+5 *g*	+20000	0x4E20	0100 1110 0010 0000
+0.5 m*g*	+2	0x0002	0000 0000 0000 0010
+0.25 m*g*	+1	0x0001	0000 0000 0000 0001
0 *g*	0	0x0000	0000 0000 0000 0000
−0.25 m*g*	−1	0xFFFF	1111 1111 1111 1111
−0.5 m*g*	−2	0xFFFE	1111 1111 1111 1110
−5 *g*	− 20000	0xB1E0	1011 0001 1110 0000

Table 11. Temperature, Twos Complement Format

Temperature	Decimal	Hex	Binary
+105°C	+1180	0x49C	XXXX 0100 1001 1100
+25.1356°C	+2	0x002	XXXX 0000 0000 0010
+25.0678°C	+1	0x001	XXXX 0000 0000 0001
+25°C	0	0x000	XXXX 0000 0000 0000
+24.9322°C	−1	0xFFF	XXXX 1111 1111 1111
+24.8644°C	−2	0xFFE	XXXX 1111 1111 1110
−40°C	−959	0xC41	XXXX 1100 0100 0001

Table 12. Analog Input, Offset Binary Format

Input Voltage	Decimal	Hex	Binary
3.3 V	4095	0xFFF	XXXX 1111 1111 1111
1 V	1241	0x4D9	XXXX 0100 1101 1001
1.6118 mV	2	0x002	XXXX 0000 0000 0010
805.9 µV	1	0x001	XXXX 0000 0000 0001
0 V	0	0x000	XXXX 0000 0000 0000

DEVICE CONFIGURATION

The control registers in Table 13 provide users with a variety of configuration options. The SPI provides access to these registers, one byte at a time, using the bit assignments in Figure 14. Each register has 16 bits, where Bits[7:0] represent the lower address, and Bits[15:8] represent the upper address. Figure 15 provides an example of writing 0x03 to Address 0x37 (SMPL_PRD[15:8]), using DIN = 0xB703. This example reduces the sample rate by a factor of eight (see Table 28).

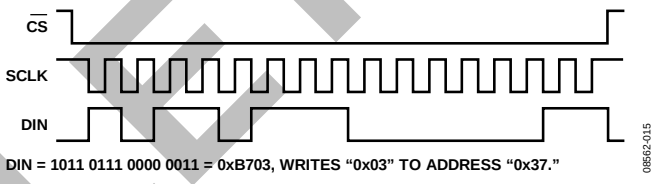

Figure 15. Example SPI Write Sequence

Dual Memory Structure

Writing configuration data to a control register updates its SRAM contents, which are volatile. After optimizing each relevant control register setting in a system, set GLOB_CMD[3] = 1 (DIN = 0xBE08) to back these settings up in nonvolatile flash memory. The flash backup process requires a valid power supply level for the entire 75 ms process time. Table 13 provides a user register memory map that includes a flash backup column. A yes in this column indicates that a register has a mirror location in flash and, when backed up properly, it automatically restores itself during startup or after a reset. Figure 16 provides a diagram of the dual-memory structure used to manage operation and store critical user settings.

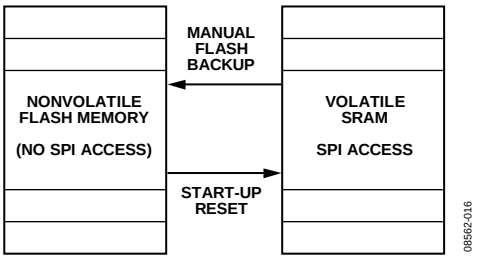

Figure 16. SRAM and Flash Memory Diagram

USER REGISTERS

Table 13. User Register Memory Map[1]

Name	R/W	Flash Backup	Address[2]	Default	Register Description	Reference
FLASH_CNT	R	Yes	0x00	N/A	Flash memory write count	Table 20
Reserved	N/A	N/A	0x02	N/A	Reserved	N/A
XGYRO_OUT	R	No	0x04	N/A	X-axis gyroscope output	Table 9
YGYRO_OUT	R	No	0x06	N/A	Y-axis gyroscope output	Table 9
ZGYRO_OUT	R	No	0x08	N/A	Z-axis gyroscope output	Table 9
XACCL_OUT	R	No	0x0A	N/A	X-axis accelerometer output	Table 10
YACCL_OUT	R	No	0x0C	N/A	Y-axis accelerometer output	Table 10
ZACCL_OUT	R	No	0x0E	N/A	Z-axis accelerometer output	Table 10
TEMP_OUT	R	No	0x10	N/A	Internal temperature output	Table 11
AUX_ADC	R	No	0x12	N/A	Auxiliary ADC output	Table 12
Reserved	N/A	N/A	0x14 to 0x19	N/A	Reserved	N/A
XGYRO_OFF	R/W	Yes	0x1A	0x0000	X-axis gyroscope bias correction factor	Table 31
YGYRO_OFF	R/W	Yes	0x1C	0x0000	Y-axis gyroscope bias correction factor	Table 31
ZGYRO_OFF	R/W	Yes	0x1E	0x0000	Z-axis gyroscope bias correction factor	Table 31
XACCL_OFF	R/W	Yes	0x20	0x0000	X-axis acceleration bias correction factor	Table 32
YACCL_OFF	R/W	Yes	0x22	0x0000	Y-axis acceleration bias correction factor	Table 32
ZACCL_OFF	R/W	Yes	0x24	0x0000	Z-axis acceleration bias correction factor	Table 32
ALM_MAG1	R/W	Yes	0x26	0x0000	Alarm 1 amplitude threshold	Table 34
ALM_MAG2	R/W	Yes	0x28	0x0000	Alarm 2 amplitude threshold	Table 35
ALM_SMPL1	R/W	Yes	0x2A	0x0000	Alarm 1 dynamic time change	Table 36
ALM_SMPL2	R/W	Yes	0x2C	0x0000	Alarm 2 dynamic time change	Table 36
ALM_CTRL	R/W	Yes	0x2E	0x0000	Alarm control	Table 37
AUX_DAC	R/W	No	0x30	0x0000	Auxiliary DAC output level setting	Table 25
GPIO_CTRL	R/W	No	0x32	0x0000	Auxiliary digital input/output control	Table 24
MSC_CTRL	R/W	Yes	0x34	0x0006	Miscellaneous control: data-ready, self-test	Table 21
SMPL_PRD	R/W	Yes	0x36	0x0001	Sample clock source, decimation rate	Table 28
SENS_AVG	R/W	Yes	0x38	0x0402	Dynamic range and digital filter control	Table 29
SLP_CTRL	W	No	0x3A	0x0000	Sleep mode control	Table 16
DIAG_STAT	R	No	0x3C	0x0000	System status (error flags)	Table 22
GLOB_CMD	R/W	No	0x3E	0x0000	System command (global)	Table 15
Reserved	N/A	N/A	0x40 to 0x51	N/A	Reserved	N/A
LOT_ID1	R	Yes	0x52	N/A	Lot Identification Code 1	Table 17
LOT_ID2	R	Yes	0x54	N/A	Lot Identification Code 2	Table 17
PROD_ID	R	Yes	0x56	0x4001	Product identification, ADIS16385	Table 19
SERIAL_NUM	R	Yes	0x58	N/A	Serial number	Table 18

[1] N/A = not applicable.
[2] Each register contains two bytes. The address of the lower byte is displayed. The address of the upper byte is equal to the address of the lower byte plus 1.

SYSTEM FUNCTIONS

The ADIS16385 provides a number of system-level controls for managing its operation, using the registers in Table 14.

Table 14. System Tool Registers

Register Name	Address	Description
MSC_CTRL	0x34	Self-test, calibration, data-ready
SLP_CTRL	0x3A	Sleep mode control
DIAG_STAT	0x3C	Error flags
GLOB_CMD	0x3E	Single-command functions
LOT_ID1	0x52	Lot Identification Code 1
LOT_ID2	0x54	Lot Identification Code 2
PROD_ID	0x56	Product identification
SERIAL_NUM	0x58	Serial number

GLOBAL COMMANDS

The GLOB_CMD register in Table 15 provides trigger bits for device reset, flash memory management, DAC control, and calibration control. Start each of these functions by writing a 1 to the assigned bit in GLOB_CMD. After completing the task, the bit automatically returns to 0. For example, set GLOB_CMD[7] = 1 (DIN = 0xBE80) to initiate a software reset, which stops the sensor operation and runs the device through its start-up sequence. Set GLOB_CMD[3] = 1 (DIN = 0xBE08) to back up the user register contents in nonvolatile flash. This sequence includes loading the control registers with the data in their respective flash memory locations prior to producing new data.

Table 15. GLOB_CMD Bit Descriptions

Bits	Description (Default = 0x0000)
[15:8]	Not used
[7]	Software reset
[6:4]	Not used
[3]	Flash update
[2]	Auxiliary DAC data latch
[1]	Factory calibration restore
[0]	Automatic bias correction

POWER MANAGEMENT

The SLP_CTRL register, in Table 16, provides two different sleep modes for system-level management: normal and timed. Set SLP_CTRL[8] = 1 (DIN = 0xBB01) to start normal sleep mode. When the device is in sleep mode, the following events can cause it to wake up: assert $\overline{CS}$ from high to low, assert $\overline{RST}$ from high to low, or cycle the power. Use SLP_CTRL[7:0] to put the device into sleep mode for a specified period. For example, SLP_CNT[7:0] = 0x64 (DIN = 0xBA64) puts the ADIS16385 to sleep for 50 seconds.

Table 16. SLP_CTRL Bit Descriptions

Bits	Description (Default = 0x0000)
[15:9]	Not used.
[8]	Normal sleep mode (1 = start sleep mode).
[7:0]	Timed sleep mode (write 0x01 to 0xFF to start). Sleep mode duration, binary, 0.5 sec/LSB.

PRODUCT IDENTIFICATION

The PROD_ID register in Table 19 contains the binary equivalent of 16,385. It provides a product-specific variable for systems that need to track this in their system software. The LOT_ID1 and LOT_ID2 registers in Table 17 combine to provide a unique, 32-bit lot identification code. The SERIAL_NUM register in Table 18 contains a binary number that represents the serial number on the device label. The assigned serial numbers in SERIAL_NUM are lot specific.

Table 17. LOT_ID1, LOT_ID2 Bit Descriptions

Bits	Description
[15:0]	Lot identification, binary code

Table 18. SERIAL_NUM Bit Descriptions

Bits	Description
[15:14]	Reserved
[13:0]	Serial number, 1 to 9999 (0x270F)

Table 19. PROD_ID Bit Descriptions

Bits	Description (Default = 0x4001)
[15:0]	Product identification = 0x4001

MEMORY MANAGEMENT

The FLASH_CNT register in Table 20 provides a 16-bit counter that helps track the number of write cycles to the nonvolatile flash memory. The flash is updated every time a manual flash update occurs. A manual flash update is initiated by the GLOB_CMD[3] bit and is also performed at the completion of the GLOB_CMD[1:0] functions (see Table 15).

Table 20. FLASH_CNT Bit Descriptions

Bits	Description
[15:0]	Binary counter

Checksum Test

Set MSC_CTRL[11] = 1 (DIN = 0xB508) to perform a checksum test of the internal program memory. This takes a summation of the internal program memory and compares it with the original summation value for the same locations (from factory configuration). Check the results in the DIAG_STAT register, which is in Table 22. DIAG_STAT[6] equals 0 if the sum matches the correct value and 1 if it does not. Make sure that the power supply is within specification for the entire 20 ms that this function takes to complete.

SELF-TEST FUNCTION

The MSC_CTRL register in Table 21 provides a self-test function for all six MEMS inertial sensors. This function allows the user to verify the mechanical integrity of each MEMS sensor. When enabled, the self-test applies an electrostatic force to each internal sensor element, which causes them to move. The movement in each element simulates its response to actual rotation/acceleration and generates a predictable electrical response in the sensor outputs. Table 1 provides the expected response for both gyroscopes and accelerometers that can help establish pass/fail limits during system-level diagnostic testing.

Table 21. MSC_CTRL Bit Descriptions

Bits	Description (Default = 0x0006)
[15:12]	Not used
[11]	Checksum memory test (cleared upon completion)[1] (1 = enabled, 0 = disabled)
[10]	Internal self-test (cleared upon completion)[1] (1 = enabled, 0 = disabled)
[9]	Not used
[8]	Manual self-test (1 = enabled, 0 = disabled)
[7]	Linear acceleration bias compensation for gyroscopes (1 = enabled, 0 = disabled)
[6]	Point of percussion, per Figure 6 (1 = enabled, 0 = disabled)
[5:3]	Not used
[2]	Data-ready enable (1 = enabled, 0 = disabled)
[1]	Data-ready polarity (1 = active high, 0 = active low)
[0]	Data-ready line select (1 = DIO2, 0 = DIO1)

[1] The bit is automatically reset to 0 after finishing the test.

There are two self-test options in the MSC-CTRL register: internal and manual. Set MSC_CTRL[10] = 1 (DIN = 0xB504) to run the internal self-test routine, which exercises all inertial sensors, measures each response, computes the response to the self-test stimulus, makes pass/fail decisions, and reports them to the error flags in DIAG_STAT[5] and DIAG_STAT[15:10]. DIAG_STAT[15:10] provide individual error flags for each inertial sensor; DIAG_STAT[5] provides a single bit for indicating a failure in any of the inertial sensors. MSC_CTRL[10] resets itself to 0 after completing the routine.

Set MSC_CTRL[8] = 1 (DIN = 0xB501) to manually activate the self-test function on all six sensors. Set MSC_CTRL[8] = 0 (DIN = 0xB500) to manually deactivate the self-test function on all six sensors. Measure the output bias for each MSC_CTRL[8] setting (0 and 1), take the difference between them, and compare this difference with the expected self-test response in Table 1.

STATUS

The DIAG_STAT register in Table 22 provides error flags for a number of functions. Each flag uses 1 to indicate an error condition and 0 to indicate a normal condition. Reading this register provides access to each flag's status and resets all of the bits to 0 for monitoring future operation. If the error condition remains, the error flag will return to 1 at the conclusion of the next sample cycle. DIAG_STAT[0] does not require a read of this register to return to 0. If the power supply voltage goes back into range, this flag clears automatically. The SPI communication error flag in DIAG_STAT[3] indicates that the number of SCLKs in a SPI sequence did not equal a multiple of 16 SCLKs.

Table 22. DIAG_STAT Bit Descriptions

Bits	Description (Default = 0x0000)
[15]	Z-axis accelerometer self-test failure (1 = fail, 0 = pass)
[14]	Y-axis accelerometer self-test failure (1 = fail, 0 = pass)
[13]	X-axis accelerometer self-test failure (1 = fail, 0 = pass)
[12]	Z-axis gyroscope self-test failure (1 = fail, 0 = pass)
[11]	Y-axis gyroscope self-test failure (1 = fail, 0 = pass)
[10]	X-axis gyroscope self-test failure (1 = fail, 0 = pass)
[9]	Alarm 2 status (1 = active, 0 = inactive)
[8]	Alarm 1 status (1 = active, 0 = inactive)
[7]	Not used
[6]	Flash test, checksum flag (1 = fail, 0 = pass)
[5]	Self-test diagnostic error flag (1 = fail, 0 = pass)
[4]	Sensor overrange (1 = overrange, 0 = normal)
[3]	SPI communication failure (1 = fail, 0 = pass)
[2]	Flash update failure (1 = fail, 0 = pass)
[1]	Not used
[0]	Power supply low (1 = VDD < 4.85 V, 0 = VDD ≥ 4.85 V)

INPUT/OUTPUT CONFIGURATION

Table 23 provides a summary of registers that provide input/output configuration and control.

Table 23. Input/Output Registers

Register Name	Address	Description
AUX_DAC	0x30	Output voltage control, AUX_DAC
GPIO_CTRL	0x32	General-purpose I/O control
MSC_CTRL	0x34	Self-test, calibration, data-ready

DATA-READY I/O INDICATOR

The factory-default setting of MSC_CTRL[2:0] (110) establishes DIO1 as a positive polarity data-ready signal. See Table 21 for additional data-ready configuration options. For example, set MSC_CTRL[2:0] = 100 (DIN = 0xB404) to change the polarity of the data-ready signal on DIO1 for interrupt inputs that require negative logic inputs for activation. The pulse width is typically between 40 µs and 80 µs.

GENERAL-PURPOSE I/O

DIO1, DIO2, DIO3, and DIO4 are configurable, general-purpose I/O lines that serve multiple purposes. The data-ready controls in MSC_CTRL[2:0] have the highest priority for configuring DIO1 and DIO2. The alarm indicator controls in ALM_CTRL[2:0] have the second-highest priority for configuring DIO1 and DIO2. The external clock control associated with SMPL_PRD[7:0] has the highest priority for DIO4 configuration (see Table 28). GPIO_CTRL in Table 24 has the lowest priority for configuring DIO1, DIO2, and DIO4 and has absolute control over DIO3.

Table 24. GPIO_CTRL Bit Descriptions

Bits	Description (Default = 0x0000)
[15:12]	Not used
[11]	General-Purpose I/O Line 4 (DIO4) data level
[10]	General-Purpose I/O Line 3 (DIO3) data level
[9]	General-Purpose I/O Line 2 (DIO2) data level
[8]	General-Purpose I/O Line 1 (DIO1) data level
[7:4]	Not used
[3]	General-Purpose I/O Line 4 (DIO4) direction control (1 = output, 0 = input)
[2]	General-Purpose I/O Line 3 (DIO3) direction control (1 = output, 0 = input)
[1]	General-Purpose I/O Line 2 (DIO2) direction control (1 = output, 0 = input)
[0]	General-Purpose I/O Line 1 (DIO1) direction control (1 = output, 0 = input)

Example I/O Configuration

For example, set GPIO_CTRL[3:0] = 0100 (DIN = 0xB204) to set DIO3 as an output signal pin and DIO1, DIO2, and DIO4 as input signal pins. Set the output on DIO3 to 1 by setting GPIO_CTRL[10] = 1 (DIN = 0xB304). Then, read GPIO_CTRL[7:0] (DIN = 0x3200) and mask off GPIO_CTRL[9:8] and GPIO_CTRL[11] to monitor the digital signal levels on DIO4, DIO2, and DIO1.

AUXILIARY DAC

The AUX_DAC register in Table 25 provides user controls for setting the output voltage on the AUX_DAC pin. The 12-bit AUX_DAC line can drive its output to within 5 mV of the ground reference when it is not sinking current. As the output approaches 0 V, the linearity begins to degrade (~100 LSB starting point). As the sink current increases, the nonlinear range increases. The DAC latch command in GLOB_CMD[2] (see Table 15) moves the values of the AUX_DAC register into the DAC input register, enabling both bytes to take effect at the same time. This prevents undesirable output levels, which reflect single-byte changes of the AUX_DAC register.

Table 25. AUX_DAC Bit Descriptions

Bits	Description (Default = 0x0000)
[15:12]	Not used
[11:0]	Data bits, scale factor = 0.8059 mV/LSB Offset binary format, 0 V = 0 LSB

Table 26. Setting AUX_DAC = 1 V

DIN	Description
0xB0D9	AUX_DAC[7:0] = 0xD9 (217 LSB)
0xB104	AUX_DAC[15:8] = 0x04 (1024 LSB)
0xBE04	GLOB_CMD[2] = 1; move values into the DAC input register, resulting in a 1 V output level

DIGITAL PROCESSING CONFIGURATION

Table 27. Digital Processing Registers

Register Name	Address	Description
SMPL_PRD	0x36	Sample rate control
SENS_AVG	0x38	Digital filtering and range control

SAMPLE RATE

The internal sampling system produces new data in the output data registers at a rate of 1024 SPS. The SMPL_PRD register in Table 28 provides two functional controls that affect sampling and register update rates. SMPL_PRD[12:8] provides a control for reducing the update rate, using an averaging filter with a decimated output. These bits provide a binomial control that divides the data rate by a factor of 2 every time this number increases by 1. For example, set SMPL_PRD[12:8] = 00100 (DIN = 0xB704) to set the decimation factor to 16. This reduces the update rate to 64 SPS and the bandwidth to 31 Hz.

Table 28. SMPL_PRD Bit Descriptions

Bits	Description (Default = 0x0001)
[15:13]	Not used
[12:8]	Average/decimation rate setting, binomial
[7:1]	Not used
[0]	Clock: 1 = internal (1024 SPS), 0 = external

INPUT CLOCK CONFIGURATION

SMPL_PRD[0] provides a control for synchronizing the internal sampling to an external clock source. Set SMPL_PRD[0] = 0 (DIN = 0xB600) to enable the external clock. See Table 2 and Figure 4 for timing information.

DIGITAL FILTERING

The SENS_AVG register in Table 29 provides user controls for the low-pass filter. This filter contains two cascaded averaging filters that provide a Bartlett window, FIR filter response (see Figure 18). For example, set SENS_AVG[2:0] = 100 (DIN = 0xB804) to set each stage to 16 taps. When used with the default sample rate of 1024 SPS and zero decimation (SMPL_PRD[12:8] = 00000), this value reduces the sensor bandwidth to approximately 20 Hz.

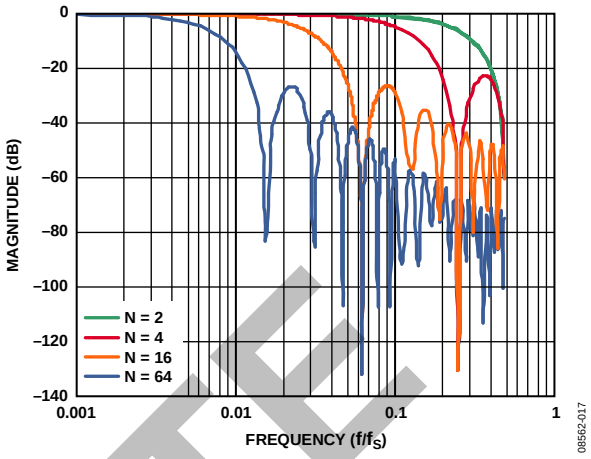

Figure 17. Bartlett Window, FIR Filter Frequency Response (Phase Delay = N Samples)

DYNAMIC RANGE

The SENS_AVG[10:8] bits provide three dynamic range settings for this gyroscope. The lower dynamic range settings (±75°/sec and ±150°/sec) limit the minimum filter tap sizes to maintain resolution. For example, set SENS_AVG[10:8] = 010 (DIN = 0xB902) for a measurement range of ±150°/sec. Because this setting can influence the filter settings, program SENS_AVG[10:8] before programming SENS_AVG[2:0] if more filtering is required.

Table 29. SENS_AVG Bit Descriptions

Bits	Description (Default = 0x0402)
[15:11]	Not used
[10:8]	Measurement range (sensitivity) selection
	100 = ±300°/sec (default condition)
	010 = ±150°/sec, filter taps ≥ 4 (Bits[2:0] ≥ 0x02)
	001 = ±75°/sec, filter taps ≥ 16 (Bits[2:0] ≥ 0x04)
[7:3]	Not used
[2:0]	Number of taps in each stage; value of B in $N_B = 2^B$

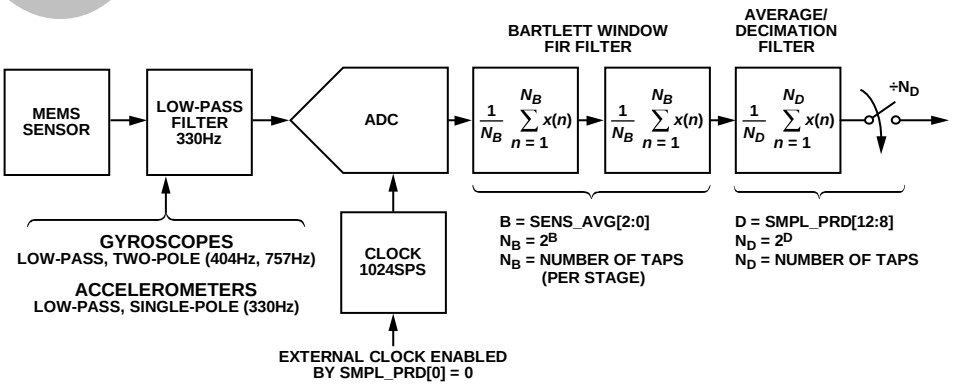

Figure 18. Sampling and Frequency Response Block Diagram

CALIBRATION

The mechanical structure and assembly process of the ADIS16385 provide excellent position and alignment stability for each sensor, even after subjected to temperature cycles, shock, vibration, and other environmental conditions. The factory calibration includes a dynamic characterization of each sensor's behavior over temperature and generates sensor-specific correction formulas. The bias correction registers in Table 30 provide users with the ability to address bias shifts that can result from mechanical stress. Figure 19 illustrates the summing function of each sensor's offset correction register.

Table 30. Registers for User Calibration

Register	Address	Description
XGYRO_OFF	0x1A	Gyroscope bias, x-axis
YGYRO_OFF	0x1C	Gyroscope bias, y-axis
ZGYRO_OFF	0x1E	Gyroscope bias, z-axis
XACCL_OFF	0x20	Accelerometer bias, x-axis
YACCL_OFF	0x22	Accelerometer bias, y-axis
ZACCL_OFF	0x24	Accelerometer bias, z-axis
GLOB_CMD	0x3E	Automatic calibration

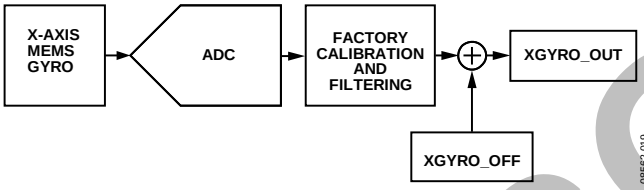

Figure 19. User Calibration, XGYRO_OFF Example

There are two options for optimizing gyroscope bias accuracy prior to system deployment: automatic bias correction (ABC) and manual bias correction (MBC).

AUTOMATIC BIAS CORRECTION (ABC)

The ABC function provides a simple measure-and-adjust function for the three gyroscope sensors. Set GLOB_CMD[0] = 1 (DIN = 0xBE01) to start the ABC function, which automatically performs the following steps to correct the bias on each gyroscope:

1. Waits for the next output register update.
2. Reads the output register of the gyroscope.
3. Multiplies the measurement by −1 to change its polarity.
4. Writes the final value into the offset register.
5. Performs a manual flash backup function to store the correction factor in nonvolatile flash memory.

The accuracy of the bias correction depends on the internal averaging time used for the data sample, which depends on the decimation setting. For example, set SMPL_PRD[15:8] = 0x10 (DIN = 0xB710) to establish a decimation rate of 2^{16}, or 65536. This establishes an averaging time of 80 seconds at a sample rate of 819.2 SPS, which results in an Allan Variance of 0.006°/sec on the x-axis and y-axis gyroscopes and 0.0016°/sec on the z-axis gyroscope.

MANUAL BIAS CORRECTION

The manual bias correction (MBC) function requires the user to collect the desired number of samples, calculate the averages to develop bias estimates for each gyroscope channel, and then write them into the bias offset registers, located in Table 31 for the gyroscopes. For example, set XGYRO_OFF = 0x1FF6 (DIN = 0x9B1F, 0x9AF6) to adjust the XGYRO_OUT offset by −0.03125°/sec (−10 LSBs). Table 32 provides a manual adjustment function for the accelerometer channels as well.

Table 31. XGYRO_OFF, YGYRO_OFF, and ZGYRO_OFF Bit Descriptions

Bits	Description (Default = 0x0000)
[15:0]	Twos complement, 0.003125°/sec per LSB. Typical adjustment range = ±102°/sec.

Table 32. XACCL_OFF, YACCL_OFF, and ZACCL_OFF Bit Descriptions

Bits	Description (Default = 0x0000)
[15:0]	Data bits. Twos complement, 0.25 mg/LSB. Typical adjustment range = ±8 *g*.

RESTORING FACTORY CALIBRATION

Set GLOB_CMD[1] = 1 (DIN = 0xBE02) to execute the factory calibration restore function. This is a single-command function, which resets each user calibration register to 0x0000 and all sensor data to 0. Then, it automatically updates the flash memory within 50 ms. See Table 15 for more information on GLOB_CMD.

POINT-OF-PERCUSSION/LINEAR-*g* COMPENSATION

Set MSC_CTRL[6] = 1 (DIN = 0xB446) to enable this feature and maintain the factory-default settings for DIO1. This feature performs a point-of-percussion translation to the point identified in Figure 6. See Table 21 for more information on MSC_CTRL. Set MSC_CTRL[7] = 1 to enable internal compensation for linear-*g* on the gyroscope bias.

ALARMS

The ADIS16385 provides two independent alarms, Alarm 1 and Alarm 2, which have a number of programmable settings. Table 33 provides a list of registers for these user settings.

Table 33. Registers for Alarm Configuration

Register	Address	Description
ALM_MAG1	0x26	Alarm 1 trigger setting
ALM_MAG2	0X28	Alarm 2 trigger setting
ALM_SMPL1	0x2A	Alarm 1 sample period
ALM_SMPL2	0x2C	Alarm 2 sample period
ALM_CTRL	0x2E	Alarm configuration

The ALM_CTRL register in Table 37 provides data source selection (Bits[15:8]), static/dynamic setting for each alarm (Bits[7:6]), trigger polarity (Bits[5:4]), data source filtering (Bit[3]), and alarm indicator signal (Bits[2:0]).

STATIC ALARM USE

The static alarms setting compares the data source selection (ALM_CTRL[15:8]) with the values in the ALM_MAGx registers in Table 34 and Table 35. The data format in these registers matches the format of the data selection in ALM_CTRL[15:8]. The ALM_CTRL[5:4] bits provide polarity settings. See Table 38, Alarm 1, for a static alarm configuration example.

Table 34. ALM_MAG1 Bit Descriptions

Bits	Description (Default = 0x0000)
[15:0]	Threshold setting; matches for format of ALM_CTRL[11:8] output register selection

Table 35. ALM_MAG2 Bit Descriptions

Bits	Description (Default = 0x0000)
[15:0]	Threshold setting; matches for format of ALM_CTRL[15:12] output register selection

DYNAMIC ALARM USE

The dynamic alarm setting monitors the data selection for a rate-of-change comparison. The rate-of-change comparison is represented by the magnitude in the ALM_MAGx registers over the time represented by the number-of-samples setting in the ALM_SMPLx registers, located in Table 36. See Table 38, Alarm 2, for a dynamic alarm configuration example.

Table 36. ALM_SMPL1 and ALM_SMPL2 Bit Descriptions

Bits	Description (Default = 0x0000)
[15:8]	Not used
[7:0]	Binary, number of samples (both 0x00 and 0x01 = 1)

ALARM REPORTING

The DIAG_STAT[9:8] bits provide error flags that indicate an alarm condition. The ALM_CTRL[2:0] bits provide controls for a hardware indicator using DIO1 or DIO2.

Table 37. ALM_CTRL Bit Descriptions

Bits	Description (Default = 0x0000)
[15:12]	Alarm 2 data source selection 0000 = disable 0001 = x-axis gyroscope output 0010 = y-axis gyroscope output 0011 = z-axis gyroscope output 0100 = x-axis accelerometer output 0101 = y-axis accelerometer output 0110 = z-axis accelerometer output 0111 = internal temperature output 1000 = auxiliary ADC input 1001 = DIAG_STAT > 0x0000
[11:8]	Alarm 1 data source selection (same as Alarm 2)
[7]	Alarm 2, dynamic/static (1 = dynamic, 0 = static)
[6]	Alarm 1, dynamic/static (1 = dynamic, 0 = static)
[5]	Alarm 2 polarity (1 = greater than, 0 = less than)
[4]	Alarm 1 polarity (1 = greater than, 0 = less than)
[3]	Data source filtering (1 = filtered, 0 = unfiltered)
[2]	Alarm indicator (1 = enabled, 0 = disabled)
[1]	Alarm indicator active polarity (1 = high, 0 = low)
[0]	Alarm output line select (1 = DIO2, 0 = DIO1)

Alarm Example

Table 38 offers an example that configures Alarm 1 to trigger when filtered ZACCL_OUT data drops below 0.7 *g*, and Alarm 2 to trigger when filtered ZGYRO_OUT data changes by more than 50°/sec over a 100 ms period, or 500°/sec^2. The filter setting helps reduce false triggers from noise and refine the accuracy of the trigger points. The ALM_SMPL2 setting of 102 samples provides a comparison period that is 99.6 ms for an internal sample rate of 1024 SPS. Because Alarm 1 is a static alarm in this example, there is no need to program ALM_SMPL1.

Table 38. Alarm Configuration Example 1

DIN	Description
0xAF36, 0xAEAF	ALM_CTRL = 0x36AF. Alarm 2: dynamic, Δ-ZGYRO_OUT (Δ-time, ALM_SMPL2) > ALM_MAG2. Alarm 1: static, ZACCL_OUT < ALM_MAG1. Use filtered data source for comparison. DIO2 output indicator, positive polarity.
0xA90F, 0xA8A0	ALM_MAG2 = 0x0FA0 (+50°/sec).
0xA70A, 0xA6F0	ALM_MAG1 = 0x0AF0 (0.7 *g*).
0xAC66	ALM_SMPL2[7:0] = 0x66 (102 samples).

APPLICATIONS INFORMATION

PROTOTYPE INTERFACE BOARD

The ADIS16385/PCBZ includes one ADIS16385BMLZ, one interface printed circuit board (PCB), and four M2×18 machine screws. The interface PCB provides larger connectors than the ADIS16385BMLZ for simpler prototyping, four tapped M2 holes for attachment of the ADIS16385BMLZ, and four holes (machine screw size M2.5 or #4) for mounting the interface PCB to a solid structure. J1 and J2 are dual-row, 2 mm (pitch) connectors that work with a number of ribbon cable systems, including 3M Part Number 152212-0100-GB (ribbon crimp connector) and 3M Part Number 3625/12 (ribbon cable).

Figure 20 provides the top-level view of the interface board. Install the ADIS16385BMLZ onto this board using the silk pattern as an orientation guide. Align the pins on the ADIS16385BMLZ to the mating connector on the interface PCB with care. Misalignment or wrong orientation can cause permanent damage. Figure 21 provides the pin assignments for J1 and J2. The pin descriptions match those listed in Table 5. The ADIS16385 does not require external capacitors for normal operation; therefore, the interface PCB does not use the C1/C2 pads.

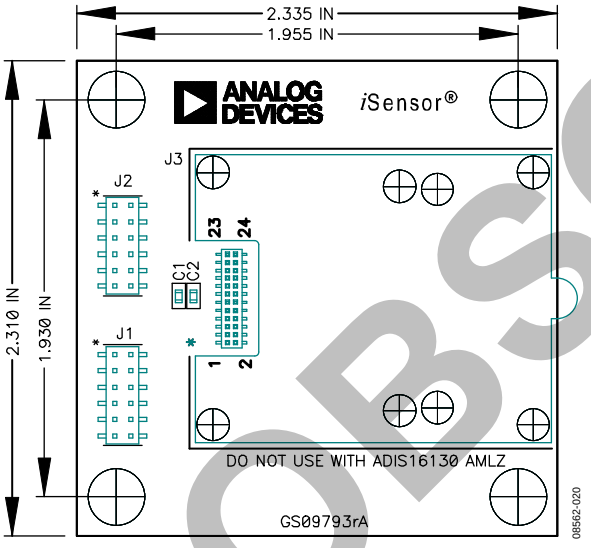

Figure 20. Physical Diagram for the ADIS16385/PCBZ

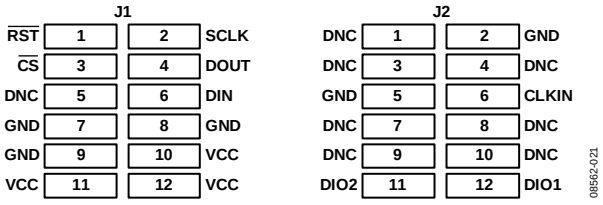

Figure 21. J1/J2 Pin Assignments

INSTALLATION TIPS

Figure 22 and Figure 23 provide the mechanical design information used for the ADIS16385/PCBZ. Use Figure 22 and Figure 23 when implementing a connector-down approach, where the mating connector and the ADIS16385BMLZ are on the same surface. When designing a connector-up system, use the mounting holes shown in Figure 22 as a guide in designing the bulkhead mounting system and use Figure 23 as a guide in developing the mating connector interface on a flexible circuit or other connector system.

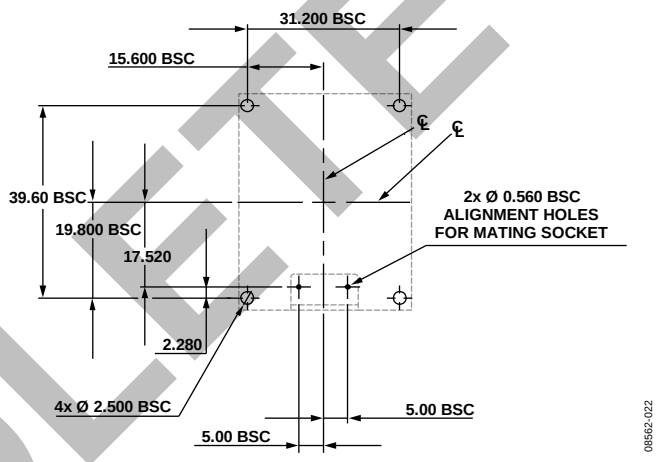

Figure 22. Suggested Mounting Hole Locations, Connector Down

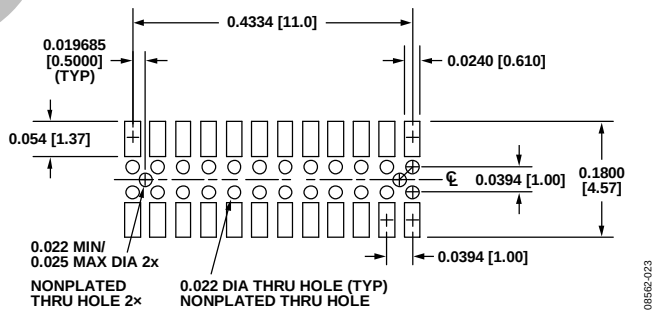

Figure 23. Suggested Layout and Mechanical Design for the Mating Connector

OUTLINE DIMENSIONS

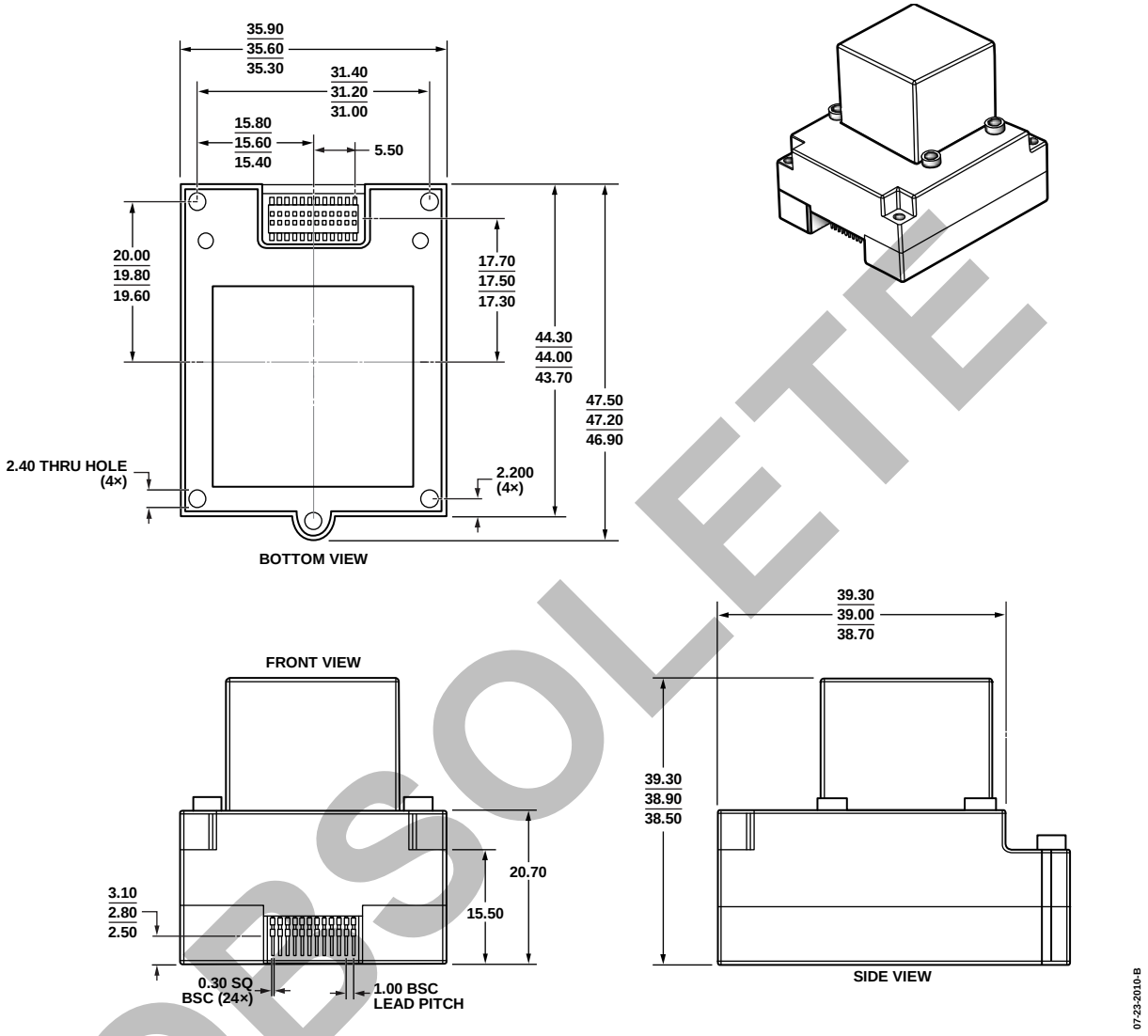

Figure 24. 24-Lead Module with Connector Interface (ML-24-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADIS16385BMLZ	−40°C to +105°C	24-Lead Module with Connector Interface	ML-24-5
ADIS16385/PCBZ		Interface PCB	

[1] Z = RoHS Compliant Part.

NOTES

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