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Low Cost, High Voltage, Programmable Gain In-Amp Using the AD5292 Digital Potentiometer and the AD8221 In-Amp

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 provides a low cost, high voltage, programmable gain instrumentation amplifier (in-amp) using the AD5292 digital potentiometer and the AD8221 in-amp.

The circuit offers 1024 different gain settings that are controllable through a digital serial peripheral interface (SPI). The ±1% resistor tolerance performance of the AD5292 provides low gain error over the full resistor range, as shown in Figure 2.

The circuit provides a high performance in-amp that delivers a high common-mode rejection ratio (CMRR) over frequency and dynamic programmable gain for both single-supply operation at +30 V and dual-supply operation at ±15 V. In addition, the AD5292 has an internal 20× programmable memory that allows the user to customize the in-amp gain at power-up.

The circuit provides accurate, low noise, high gain and is well suited for signal instrumentation conditioning, precision data acquisition, biomedical analysis, and aerospace instrumentation.

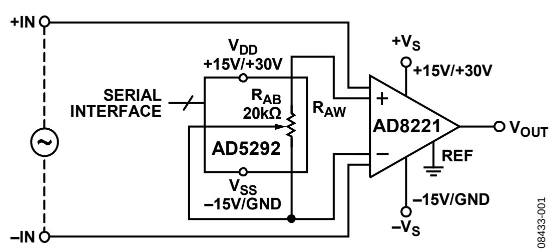

Figure 1. Programmable Gain In-Amp (Simplified Schematic, All Connections Not Shown)

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REVISION HISTORY

8/2018—Rev. A to Rev. B

Document Title Changed From CN0114 to AN-1578 .... Universal
Changes to Figure 1 1
Changes to Circuit Description Section 3

3/2010—Rev. 0 to Rev. A

Changes to Circuit Function and Benefits Section 1

8/2009—Revision 0: Initial Version

CIRCUIT DESCRIPTION

This circuit employs the AD5292 digital potentiometer in conjunction with the AD8221 in-amp, providing an overall low cost, high voltage, programmable gain in-amp.

The differential input signal, +IN and −IN, is amplified by the AD8221. The in-amp offers accuracy, low noise, high CMRR, and high slew rate.

The maximum circuit gain (G) is defined in Equation 1, where R_{AW_MIN} is the wiper resistance of the AD5292 in the rheostat mode and represents the minimum value of the gain setting resistance (100 Ω).

$$G = 1 + \frac{49.4\ \text{k}\Omega}{R_{AB}} \leq 1 + \frac{49.4\ \text{k}\Omega}{R_{AW\_MIN}} \leq 500 \quad (1)$$

where R_{AB} is the total resistance across the A and B terminals of the AD5292 in rheostat mode.

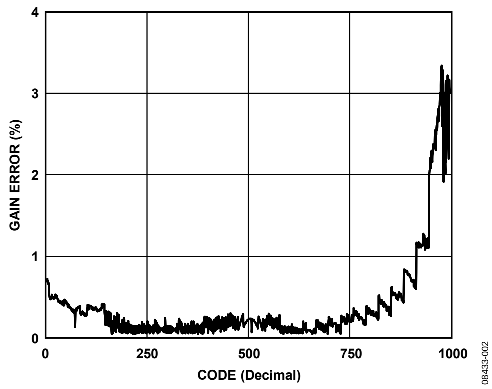

Figure 2. Gain Error vs. Code

The circuit gain formula for any particular AD5292 resistance can be calculated with the following equation:

$$G = 1 + \frac{49.4\ \text{k}\Omega}{(1024 - D) \times R_{AB} / 1024} \quad (2)$$

where *D* is the decimal code.

Equation 2 is plotted in Figure 3 as a function of the decimal code.

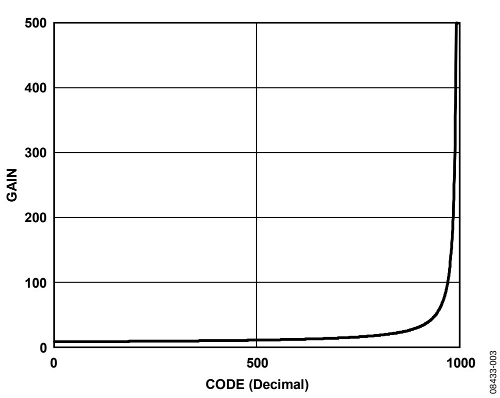

Figure 3. Gain vs. Decimal Code

The maximum current allowed through the AD5292 is ±3 mA, which limits the allowable circuit gain as a function of differential input voltage.

Equation 3 shows the maximum gain limit as a function of the differential input voltage (V_{IN}). This equation is derived by substituting $R_{AB} = V_{IN}/3$ mA into Equation 1. The result of Equation 3 is plotted in Figure 4.

$$G \leq 1 + \frac{148}{V_{IN}} \quad (3)$$

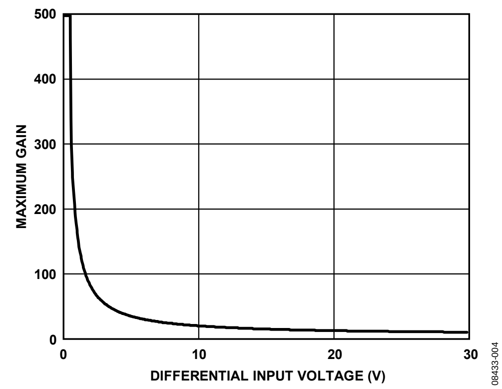

Figure 4. Allowable Gain vs. Differential Input Voltage

Equation 1 limits the maximum circuit gain to 500. Equation 2 can be solved for D, yielding Equation 4, which calculates the minimum allowable resistance (in terms of the digital code) in the AD5292 without exceeding the current limit.

$$D \geq 1024 - \left(\frac{49.4\ \text{k}\Omega \times 1024}{R_{AB} \times (G - 1)} \right) \quad (4)$$

where:
D is the code loaded in the digital potentiometer.
G is the maximum gain calculated from Equation 3.

When the input to the circuit is an ac signal, the parasitic capacitances in the digital potentiometer can cause a reduction in the maximum AD8221 bandwidth. A gain and phase plot is shown in Figure 5.

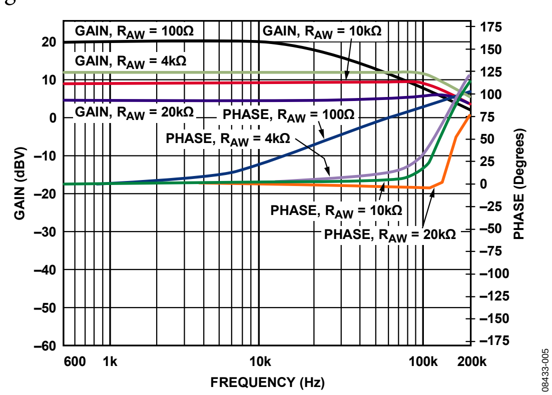

Figure 5. Gain and Phase vs. Frequency (Vertical Scale Compressed to Show All Gain Curves)

The AD5292 has a 20× programmable memory, which allows presetting the output voltage in a specific value at power-up.

Excellent layout, grounding, and decoupling techniques must be used to achieve the desired performance from the circuits discussed in this application note (see MT-031 Tutorial and MT-101 Tutorial). As a minimum, use a 4-layer printed circuit board (PCB) with one ground plane layer, one power plane layer, and two signal layers.

COMMON VARIATIONS

The AD5291 (8 bits with 20× programmable power-up memory) and the AD5293 (10 bits, no power-up memory) are both ±1% tolerance digital potentiometers that are suitable for this application.

REFERENCE

MT-031 Tutorial. *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*. Analog Devices.

MT-032 Tutorial. *Ideal Voltage Feedback (VFB) Op Amp*. Analog Devices.

MT-061 Tutorial *Instrumentation Amplifier (In-Amp) Basics*. Analog Devices.

MT-087 Tutorial. *Voltage References*. Analog Devices.

MT-091 Tutorial. *Digital Potentiometers*. Analog Devices.

MT-095 Tutorial. *EMI, RFI, and Shielding Concepts*. Analog Devices.

MT-101 Tutorial. *Decoupling Techniques*. Analog Devices.

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