

# UM2167 User manual

## OrCAD PSpice model usage instructions

### Introduction

This document describes how to use ST's PSpice models available for SMPS devices. The models are useable in the OrCAD system environment of Cadence Design Systems and will not work in other simulation platforms. Furthermore, we recommend using the latest version of OrCAD to avoid convergence problems and speed up the simulation.

PSpice models describe the characteristics of typical devices and don't guarantee the absolute representation of product specifications and operating characteristics; the datasheet is the only document providing product specifications.

Although simulation is a very important tool to evaluate the device's performance, the exact device's behavior in all situations is not predictable, therefore the final laboratory test is necessary.

### **1 PSpice models – instructions to simulate**

The model is included in a zip package that contains two files:

- "<DEVICE\_NAME>.OLB", the symbol to place in the schematic
- "<DEVICE\_NAME>.LIB", the library containing the actual implementation of the model

To use the model, unzip the package and add the library "<DEVICE\_NAME>.OLB" to your OrCAD project, as illustrated in the following figure: click the button highlighted by the red circle and browse to search the library you want to add.



Figure 1: How to add a library to an OrCAD project

Then, select the part of interest from the "Part List" and place it on the schematic as shown in the following figure.



**PSpice** models – instructions to simulate



Then, create or open your simulation profile (1), go to "Configuration Files" (2), select the category "Library" (3), browse and search the file <DEVICE\_NAME>.lib (4) and click to "Add to Design" (5), as shown in the following figure.







 Before starting the simulation, make sure that the option "Initialize all flip-flops" is set to "0" as shown in the following figure: in your simulation profile go to "Options" tab, select the Category "Gate-level Simulation" and select "0" in the dropdown list "Initialize all flip-flops to:".

🚚 Simulation Settings - aa 🛛 🔍 🔀					
General Analysis Configura	ation Files Options Data Collection Probe Window				
<u>Category:</u> Analog Simulation Gate-level Simulation Output file	Timing Mode   ○ Minimum   ● Iypical   ○ Maximum   ○ Worst-case (min/max)   □ Suppress simulation error messages in waveform data file.   Initialize all flip-flops to:   □    □    □    □    □    □    □    □    □    □    □    □    □    □    □    □    □    □    □				
	Advanced Options <u>R</u> eset				
OK Cancel Apply Help					

#### Figure 4: How set the "Initialize all flip-flops" to 0

- Almost all our converter models need to detect a rising edge of the input voltage to start the power-up sequence. For this reason, do not use a VDC component as VIN source but a VPULSE or a VPWL.
- In case you should experience convergence problems, try to play around with the "Analog Simulation" options of your simulation profile. We suggest to apply the following changes (sorted by priority):
  - Change the parameter ABSTOL from 1.0p to 1.0n.
  - Increase the value of the parameter ITL4 from 10 to 50 or 100.
  - Increase the Speed Level from 3 to 4 or 5.
  - Set the option "Auto Convergence".



#### Important notes

Figure 5: Analog Simulation options tab

					AutoConverge Options	
General Analysis Configu	ration Files Options Data Collection	Probe Win	ndow			
Category: Analog Simulation	Relative accuracy of V's and I's:	0.001		(.OPTION) (RELTOL)	AutoConverge	Relaxed limit:
Gate-level Simulation Output file	Best accuracy of voltages:	-	volts	(VNTOL)		
	Best accuracy of currents:	1.0p	amps	(ABSTOL)	₩ m1	1000
Speed Level 3	Best accuracy of charges:		coulombs	(CHGTOL)	I III.2	1000
Use Speed Level=0 for higher accuracy and compatibility with previous PSpice Version.	Minimum conductance for any <u>b</u> ranch: DC and bias "blind" iteration limit:	1.0E-12 150	1/ohm	(GMIN) (ITL1)	<b>₩</b> m.4	1000
	DC and bias "best guess" iteration limit:			(ITL2)	RELTOL	0.05
	Iransient time point iteration limit:	10		(ITL4)	ABSTOL	1.0E-6
For better simulation performance, do not use high ITL4 for Speed Level	Default nominal temperature: Number of Threads (Maximum is 4)	27.0 0	°C	(TNOM) (THREADS)	VNTOL	.001
> 0.	Advanced Convergence			(ADVCONV)	PIVTOL	1.0E-10
	Use preordering to reduce matrix fil- AutoConverge		(l ed <u>O</u> ptions	PREORDER)	I Restart	cel Reset
	OK Cancel	AP		Help	OK Can	Reset



# 3 Revision history

Table 1: Document revision history

Date	Version	Changes
14-Mar-2017	1	Initial release.
11-Apr-2017	2	Updated Figure 3: "How to add the reference to the model to the simulation profile" (replaced by new figure) and its description.



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