AO4821L

12V Dual P-Channel MOSFET

General Description

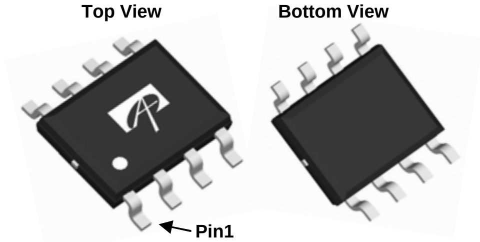
The AO4821L uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch.

Product Summary

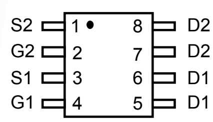
V_{DS}	-12V
I_D (at V_{GS}=-4.5V)	-9A
$R_{DS(ON)}$ (at V_{GS}=-4.5V)	< 19mΩ
$R_{DS(ON)}$ (at V_{GS} =-2.5V)	< 24mΩ
$R_{DS(ON)}$ (at V_{GS} =-1.8V)	< 30mΩ

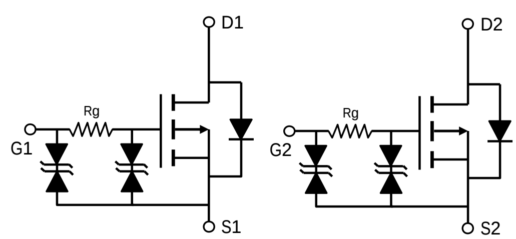
SOIC-8

Top View Bottom View



Top View





Absolute Maximum Ratings T_A=25°C unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	-12	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current	T_A=25°C	I_D	-9	A
	T_A=70°C		-7	
Pulsed Drain Current [C]		I_{DM}	-60	
Power Dissipation [B]	T_A=25°C	P_D	2	W
	T_A=70°C		1.28	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	48	62.5	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		74	90	°C/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	32	40	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V		-12			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-12V, V_{GS}=0V				-1	µA
			T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±8V				±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA		-0.35	-0.53	-0.85	V
$I_{D(ON)}$	On state drain current	V_{GS}=-4.5V, V_{DS}=-5V		-60			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-4.5V, I_D=-9A			16	19	mΩ
			T_J=125°C		22	27	
		V_{GS}=-2.5V, I_D=-8A			19	24	mΩ
		V_{GS}=-1.8V, I_D=-6A			23	30	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-9A			45		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V			-0.56	-1	V
I_S	Maximum Body-Diode Continuous Current					-3	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-6V, f=1MHz		1390	1740	2100	pF
C_{oss}	Output Capacitance			230	334	435	pF
C_{rss}	Reverse Transfer Capacitance			120	200	280	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		0.9	1.3	1.7	kΩ
SWITCHING PARAMETERS							
Q_g(4.5V)	Total Gate Charge	V_{GS}=-4.5V, V_{DS}=-6V, I_D=-9A		15	19	23	nC
Q_{gs}	Gate Source Charge			3.6	4.5	5.4	nC
Q_{gd}	Gate Drain Charge			3	5.3	7.4	nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-4.5V, V_{DS}=-6V, R_L=0.67Ω, R_{GEN}=3Ω			240		ns
t_r	Turn-On Rise Time				580		ns
$t_{D(off)}$	Turn-Off DelayTime				7		µs
t_f	Turn-Off Fall Time				4.2		µs
t_{rr}	Body Diode Reverse Recovery Time	I_F=-9A, dI/dt=500A/µs		18	22	26	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-9A, dI/dt=500A/µs		14	17	20	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initialT_J=25°C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

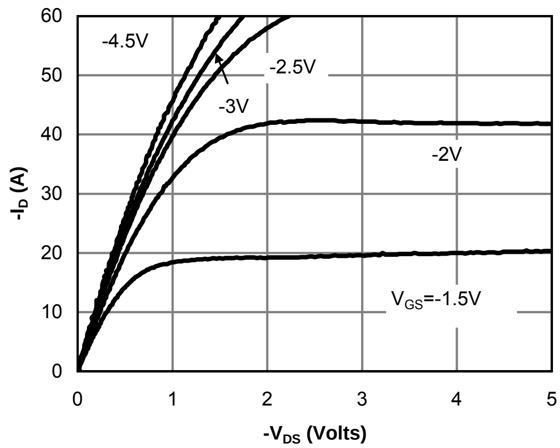


Fig 1: On-Region Characteristics (Note E)

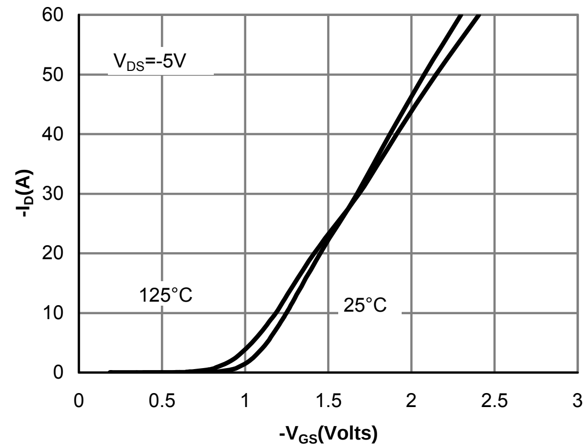


Figure 2: Transfer Characteristics (Note E)

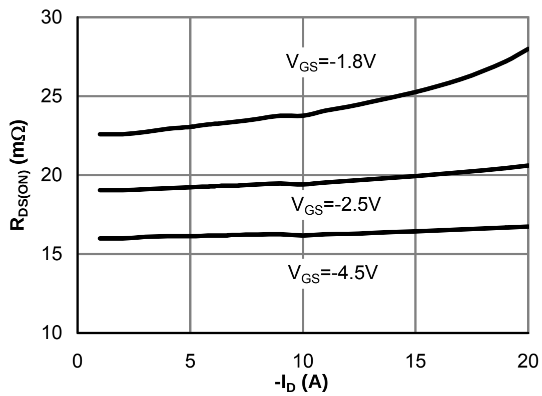


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

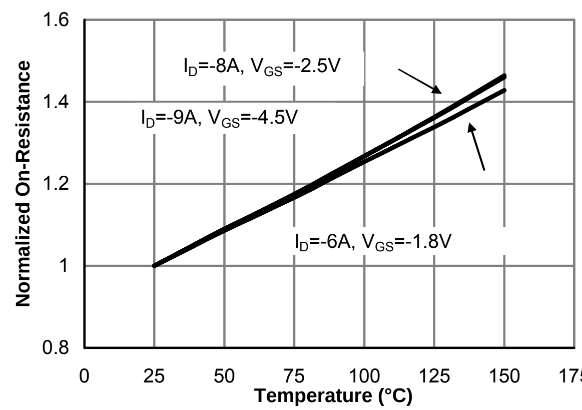


Figure 4: On-Resistance vs. Junction Temperature (Note E)

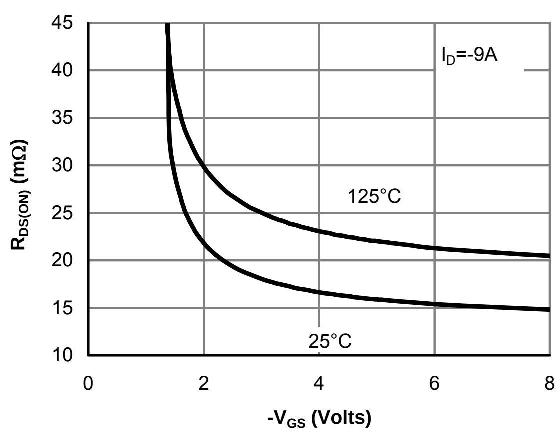


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

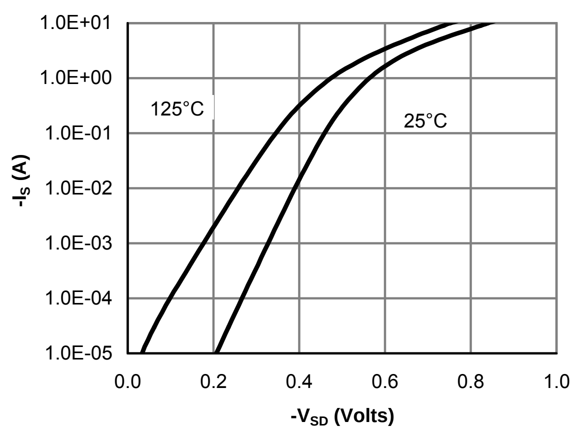


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

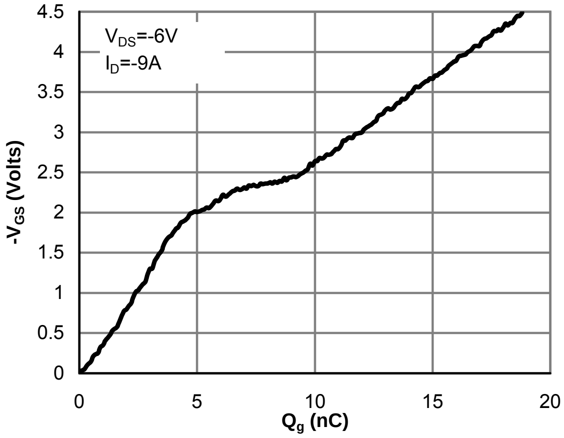


Figure 7: Gate-Charge Characteristics

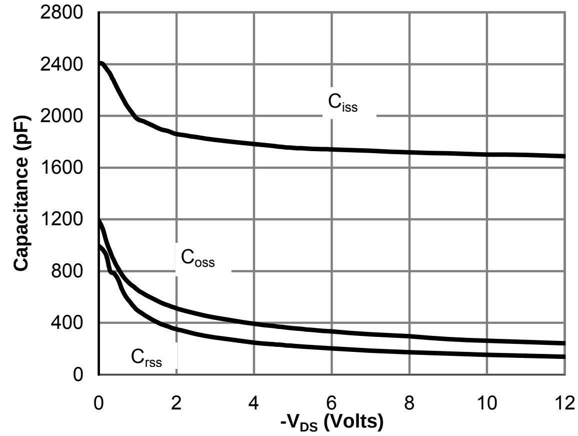


Figure 8: Capacitance Characteristics

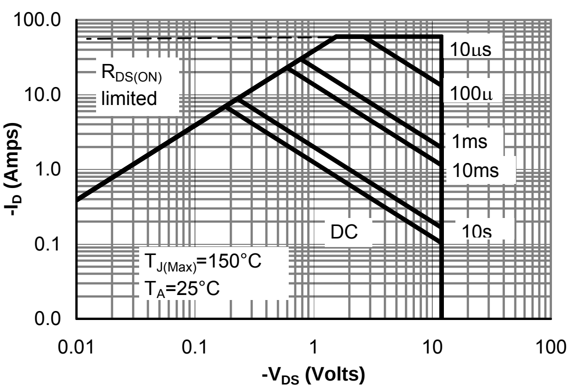


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

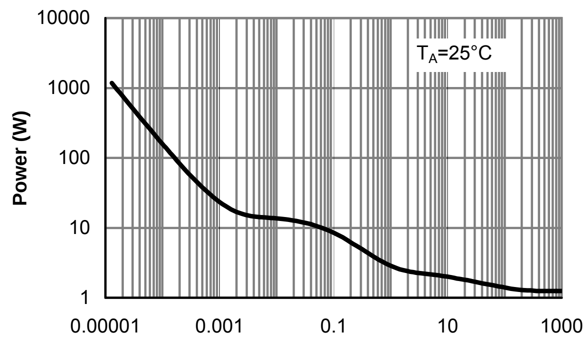


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

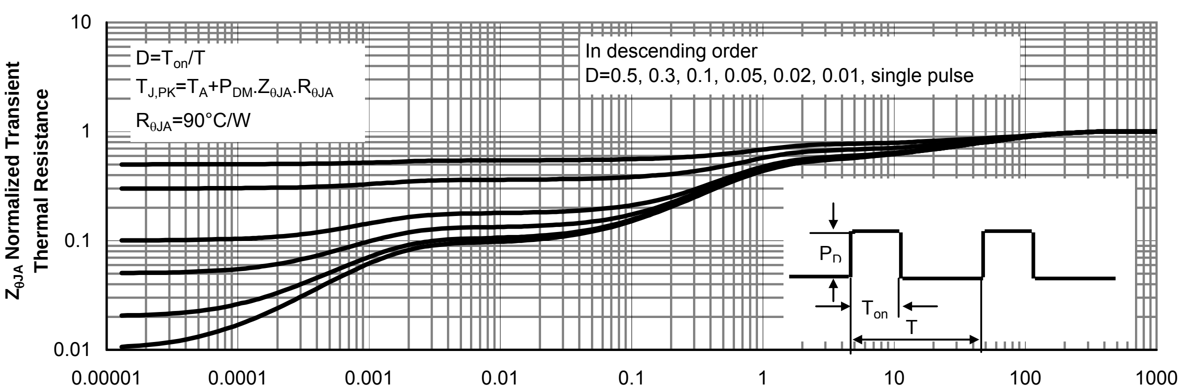
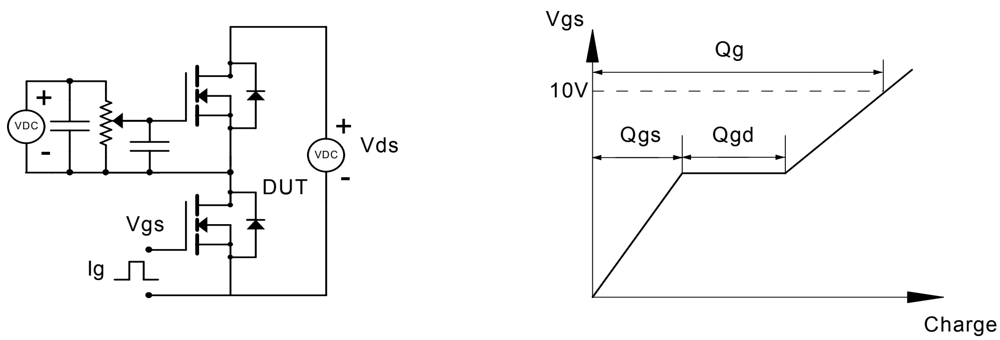
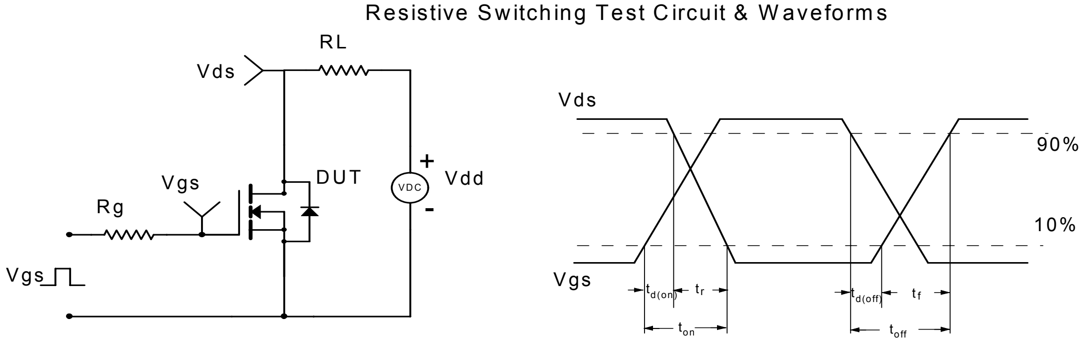


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms