GV7600

Aviia™ Transmitter

Key Features

- Serial digital video transmitter for standard and high definition component video:
  - SD 525i and 625i
  - HD 720p 24, 25, 30, 50 and 60
  - HD 1080i 50, 60
  - HD 1080p 24, 25, 30, 50 and 60
- Supports 8-bit, 10-bit or 12-bit component digital video:
  - RGB or YCbCr 4:4:4 sampled
  - YCbCr 4:2:2 or 4:2:0 sampled
- Single 75Ω coaxial cable driver output
- Integrated audio embedder for the carriage of up to 8 channels of 48kHz digital audio
- Asynchronous Serial Interface (ASI) for transmission of IEC 13818-1 compliant transport streams
- Ancillary (ANC) data insertion
- User selectable processing features, including:
  - Timing Reference Signal (TRS) insertion
  - Programmable ANC data insertion
  - Illegal video code word re-mapping
- 4-wire Gennum Serial Peripheral Interface (GSPI) for external host command and control
- Dedicated JTAG test interface
- 1.2V core and 3.3V analog voltage power supplies
- 1.8V or 3.3V selectable digital I/O power supply
- Small footprint 100-BGA (11mm x 11mm)
- Low power operation, typically 400mW
- Pb-free and RoHS compliant

Applications

- Industrial & professional cameras
- Digital video recorders (DVR)
- Video servers
- Video mixers and switchers
- Camcorders

Description

The GV7600 is a serial digital video transmitter for standard and high definition component video. With integrated cable driving technology, the GV7600 is capable of transmitting digital video at 270Mb/s, 1.485Gb/s and 2.97Gb/s over 75Ω coaxial cable. The device provides a complete transmit solution for the transmission of both interlaced and progressive component digital video, up to 1920 x 1080, in coaxial cable-based video systems.

Using the GV7600 with the complete Aviia transmitter reference design, it is possible to implement an all-digital, bi-directional multimedia interface over coax. This interface allows both DC power and a bi-directional, half-duplex, auxiliary data interface, up to 1Mb/s, to be carried over the same single, robust and cost effective coaxial cable as the high-speed serial digital video.

The GV7600 includes a broad range of user-selectable processing features, such as Timing Reference Signal (TRS) insertion, illegal code word re-mapping, and ancillary data packet insertion. The content of ancillary data packets can be programmed via the host interface. Device configuration and status reporting is accomplished via the Gennum Serial Peripheral Interface (GSPI). Alternatively, many processing features and operational modes can be configured directly through external pin settings.

The device supports both 8-bit, 10-bit and 12-bit video data input, for RGB or YCbCr 4:4:4, and YCbCr 4:2:2 or 4:2:0. A configurable 20-bit wide parallel digital video input bus is provided, with associated pixel clock and timing signal inputs. The GV7600 supports direct interfacing of ITU-R BT.656 SD formats, and HD formats conforming to ITU-R BT.709 and BT.1120-6 for 1125-line formats, and SMPTE 296M for 750-line formats. The device may also be configured to accepts CEA-861 timing.

The GV7600 audio embedding function allows the carriage of up to 8 channels of serial digital audio within the ancillary data space of the video data stream. The input audio signal formats supported by the device include AES/EBU for professional applications, S/PDIF, and I^2S. 16-bit, 20-bit and 24-bit audio formats are supported at

48kHz synchronous-to-video for SD video formats and 48kHz synchronous or asynchronous for HD formats. Additional audio processing features include: individual channel enabling, audio group selection, group replacement, channel swapping and audio channel status insertion.

The GV7600 supports an Asynchronous Serial Interface (ASI), to carry compressed audio and video transport streams, conforming to IEC 13818-1, at 270Mb/s. Transport stream data is input to the device at a synchronous 27MHz clock rate. The device will automatically 8b/10b encode the data, prior to serialization.

Packaged in a space saving 100-BGA, the GV7600 is ideal for designs where high-density component placement is required. Typically requiring only 400mW power, the device can be used as a high bandwidth alternative to analog composite or component video interfaces, providing a high quality, all-digital, long reach video transmit solution.

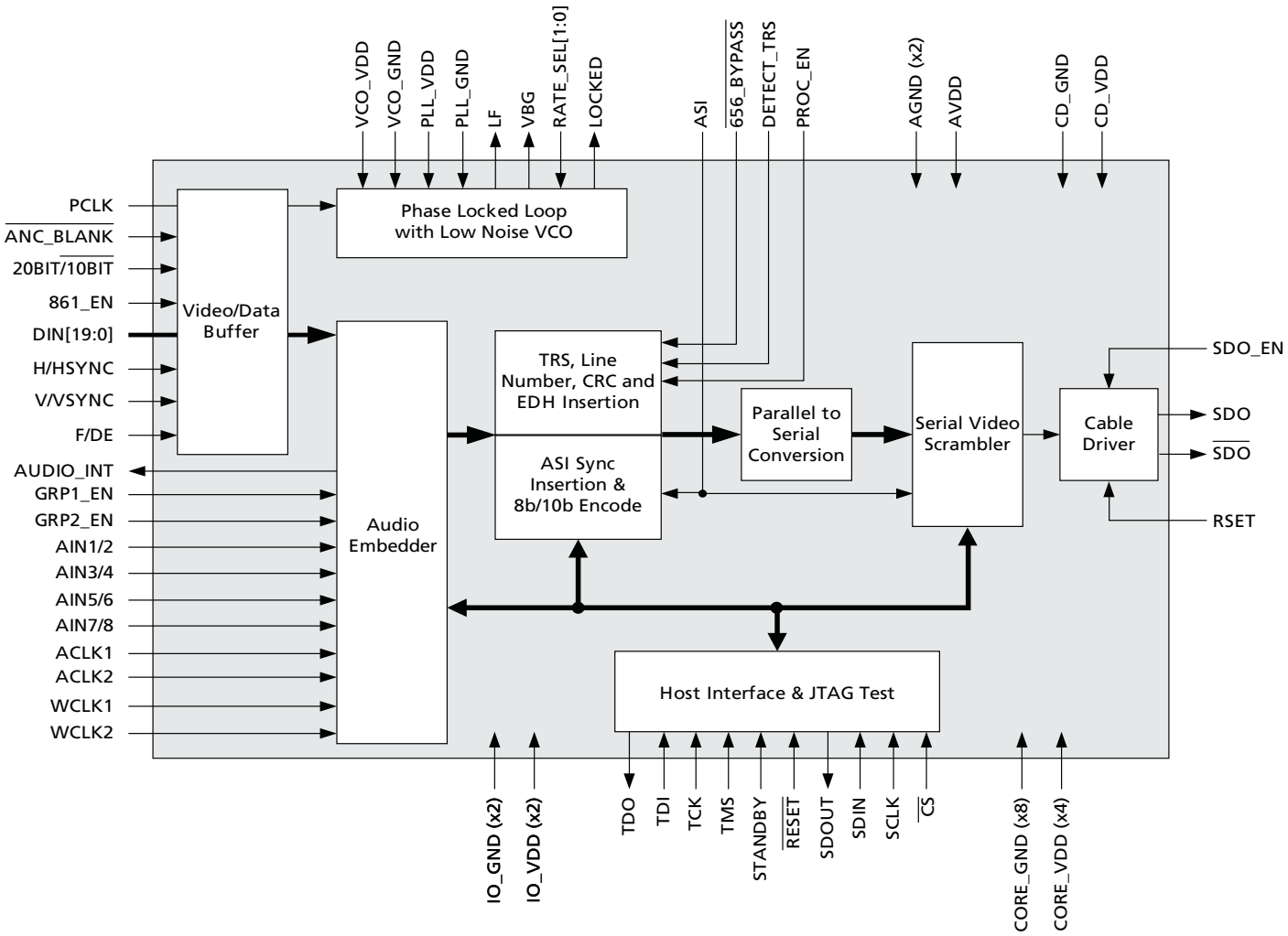

Figure A: GV7600 Functional Block Diagram

Revision History

Version	ECR	Date	Changes and / or Modifications
8	019059	April 2014	Updated Figure 6-1: GV7600 Package Dimensions
7	153723	March 2010	Changes to addresses 040h -> 13Fh in Table 4-29: Video Core Configuration and Status Registers.
6	153582	February 2010	Added analog input absolute maximum ratings to Table 2-1: Absolute Maximum Ratings.
5	152573	September 2009	Changed Reset Pulse Width from 10ms to 1ms.
4	152157	June 2009	Changed Figure 4-54 and 6.3 Marking Diagram.
3	151832	May 2009	Re-ordered the DIN[19:10] & DIN[9:0] in Table 1-1 to reflect the pin names. Added Device Latency in Table 2-4. Changed description in Section 4.7.2. Changed Figure 4-47. Changed descriptions to address 40Bh in Table 4-30 & address 80Ah in Table 4-31.
2	151644	April 2009	Changed 4.8.1 Ancillary Data Insertion Operating Modes and their registers.
1	151321	February 2009	Altered Parallel Video Data Inputs DIN[9:0] & DIN[9:0] section. Changed table in Full HD Input Formats section. Added Aviia 20-bit Mapping Structure for 1280x720 100/120Hz Progressive 4:2:2 ($Y'C'_BC'_R$) 8/10-bit Signals. Added section: Video Format & Bandwidth Requirements. Changed/Added to H:V:F Timing diagrams. Added GSPI timing delay values. Added Index.
0	150962	December 2008	New document.

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1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	DIN17	DIN18	F/DE	H/ HSYNC	CORE_ VDD	PLL_ VDD	LF	VBG	RSV	AVDD
B	DIN15	DIN16	DIN19	PCLK	CORE_ GND	PLL_ VDD	VCO_ VDD	VCO_ GND	AGND	AGND
C	DIN13	DIN14	DIN12	V/ VSYNC	CORE_ GND	PLL_ GND	PLL_ GND	PLL_ GND	CD_ GND	SDO
D	DIN11	DIN10	STAND BY	SDO_ EN	RSV	RSV	RSV	RSV	CD_ GND	$\overline{\text{SDO}}$
E	CORE_ VDD	CORE_ GND	RATE_ SEL0	RATE_ SEL1	CORE_ GND	CORE_ GND	TDI	TMS	CD_ GND	CD_ VDD
F	DIN9	DIN8	DETECT _TRS	RSV	CORE_ GND	CORE_ GND	RSV	TDO	CD_ GND	RSET
G	IO_VDD	IO_GND	861_EN	$\overline{\text{20BIT}}$/ 10BIT	ASI	$\overline{\text{656}}$_ $\overline{\text{BYPASS}}$	PROC _EN	$\overline{\text{RESET}}$	CORE_ GND	CORE_ VDD
H	DIN7	DIN6	$\overline{\text{ANC}}$_ $\overline{\text{BLANK}}$	LOCKED	GRP2_ EN	GRP1_ EN	AUDIO _INT	RSV	IO_ GND	IO_ VDD
J	DIN5	DIN4	DIN1	AIN5/6	WCLK2	AIN1/2	WCLK1	TCK	SDOUT	SCLK
K	DIN3	DIN2	DIN0	AIN7/8	ACLK2	AIN3/4	ACLK1	CORE_ VDD	$\overline{\text{CS}}$	SDIN

Figure 1-1: GV7600 Pin Assignment

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description	
B3, A2, A1, B2, B1, C2, C1, C3, D1, D2	DIN[19:10]		Input	PARALLEL DATA BUS Signal levels are LVCMOS / LVTTL compatible.	
				20-bit mode 20BIT/$\overline{10BIT}$ = HIGH	Data Stream 1/Luma data input in video mode ($\overline{656\_BYPASS}$ = HIGH) Data input in data through mode ($\overline{656\_BYPASS}$ = LOW)
				10-bit mode 20BIT/$\overline{10BIT}$ = LOW	Multiplexed Data Stream 1/Luma and Data Stream 2/Chroma data input in video mode ($\overline{656\_BYPASS}$ = HIGH) Data input in data through mode ($\overline{656\_BYPASS}$ = LOW) Transport stream data input in ASI mode ($\overline{656\_BYPASS}$ = LOW) (ASI = HIGH)
A3	F/DE	Synchronous with PCLK	Input	PARALLEL DATA TIMING. Signal levels are LVCMOS / LVTTL compatible. 861_EN = LOW: Used to indicate the ODD / EVEN field of the video signal when DETECT_TRS is set LOW. The device sets the F bit in all outgoing TRS signals for the entire period that the F input signal is HIGH (PROC_EN must also be HIGH). The F signal should be set HIGH for the entire period of field 2 and should be set LOW for all lines in field 1 and for all lines in progressive scan systems. The F signal is ignored when DETECT_TRS = HIGH. 861_EN = HIGH: The DE signal is used to indicate the active video period when DETECT_TRS is LOW. DE is HIGH for active data and LOW for blanking. See Section 4.3.1 and Section 4.3.2 for timing details. The DE signal is ignored when DETECT_TRS = HIGH.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
A4	H/HSYNC	Synchronous with PCLK	Input	PARALLEL DATA TIMING. Signal levels are LVCMOS / LVTTL compatible. 861_EN is LOW: The H signal is used to indicate the portion of the video line containing active video data, when DETECT_TRS is set LOW. Active Line Blanking The H signal should be LOW for the active portion of the video line. The signal goes LOW at the first active pixel of the line, and then goes HIGH after the last active pixel of the line. The H signal should be set HIGH for the entire horizontal blanking period, including both EAV and SAV TRS words, and LOW otherwise. TRS Based Blanking (H_CONFIG = 1_h) The H signal should be set HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS ID words, and LOW otherwise. 861_EN = HIGH: The HSYNC signal indicates horizontal timing. See Section 4.3.1. When DETECT_TRS is HIGH, this pin is ignored at all times. If DETECT_TRS is set HIGH and 861_EN is set HIGH, the DETECT_TRS feature takes priority.
A5, E1, G10, K8	CORE_VDD		Input Power	Power supply connection for digital core logic. Connect to 1.2V DC digital.
A6, B6	PLL_VDD		Input Power	Power supply pin for PLL. Connect to 1.2V DC analog.
A7	LF		Analog Output	Loop Filter component connection.
A8	VBG		Output	Bandgap voltage filter connection.
A9, D6, D7, D8, F4	RSV		–	These pins are reserved and should be left unconnected.
A10	AVDD		Input Power	VDD for sensitive analog circuitry. Connect to 3.3VDC analog.
B4	PCLK		Input	PARALLEL DATA BUS CLOCK. Signal levels are LVCMOS / LVTTL compatible. Full HD 20-bit mode: PCLK @ 148.5MHz Full HD 10-bit mode DDR: PCLK @ 148.5MHz HD 20-bit mode: PCLK @ 74.25MHz HD 10-bit mode: PCLK @ 148.5MHz SD 20-bit mode: PCLK @ 13.5MHz SD 10-bit mode: PCLK @ 27MHz ASI mode: PCLK @ 27MHz

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
B5, C5, E2, E5, E6, F5, F6, G9	CORE_GND		Input Power	GND connection for digital logic. Connect to digital GND.
B7	VCO_VDD		Input Power	Power pin for VCO. Connect to 1.2V DC analog followed by an RC filter. VCO_VDD is nominally 0.7V.
B8	VCO_GND		Input Power	Ground connection for VCO. Connect to analog GND.
B9, B10	AGND		Input Power	GND pins for sensitive analog circuitry. Connect to analog GND.
C4	V/VSYNC	Synchronous with PCLK	Input	PARALLEL DATA TIMING. Signal levels are LVCMOS / LVTTL compatible. 861_EN = LOW: The V signal is used to indicate the portion of the video field/frame that is used for vertical blanking, when DETECT_TRS is set LOW. The V signal should be set HIGH for the entire vertical blanking period and should be set LOW for all lines outside of the vertical blanking interval. The V signal is ignored when DETECT_TRS = HIGH. 861_EN = HIGH: The VSYNC signal indicates vertical timing. See 4.9.2 Ancillary Data Blanking for timing details. The VSYNC signal is ignored when DETECT_TRS = HIGH.
C6, C7, C8	PLL_GND		Input Power	Ground connection for PLL. Connect to analog GND.
C9, D9, E9, F9	CD_GND		Input Power	Ground connection for the serial digital cable driver. Connect to analog GND.
C10, D10	SDO, $\overline{\text{SDO}}$		Output	Serial Data Output Signal. Serial digital output signal operating at 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485 /1.001Gb/s or 270Mb/s. The slew rate of the output is automatically controlled according to the setting of the RATE_SEL0 and RATE_SEL1 pins.
D3	STANDBY		Input	Power Down input. HIGH to power down device.
D4	SDO_EN		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Used to enable or disable the serial digital output stage. When SDO_EN is LOW, the serial digital output signals SDO and $\overline{\text{SDO}}$ are disabled and become high impedance. When SDO_EN is HIGH, the serial digital output signals SDO and $\overline{\text{SDO}}$ are enabled.
D5, F7, H8	RSV		–	These pins are reserved and should be connected to CORE_GND.

Table 1-1: Pin Descriptions (Continued)

<table>
<tr><th>Pin Number</th><th>Name</th><th>Timing</th><th>Type</th><th>Description</th></tr>
<tr><td>E3, E4</td><td>RATE_SEL0,
RATE_SEL1</td><td></td><td>Input</td><td>CONTROL SIGNAL INPUT.
Signal levels are LVCMOS/LVTTL compatible.
Used to configure the operating data rate.
<table><tr><th>RATE_SEL0</th><th>RATE_SEL1</th><th>Data Rate</th></tr><tr><td>0</td><td>0</td><td>1.485 or 1.485/1.001Gb/s</td></tr><tr><td>0</td><td>1</td><td>2.97 or 2.97/1.001Gb/s</td></tr><tr><td>1</td><td>X</td><td>270Mb/s</td></tr></table></td></tr>
<tr><td>E7</td><td>TDI</td><td></td><td>Input</td><td>COMMUNICATION SIGNAL INPUT.
Signal levels are LVCMOS/LVTTL compatible.
Dedicated JTAG pin.
Test data in.
This pin is used to shift JTAG test data into the device.</td></tr>
<tr><td>E8</td><td>TMS</td><td></td><td>Input</td><td>COMMUNICATION SIGNAL INPUT.
Signal levels are LVCMOS/LVTTL compatible.
Dedicated JTAG pin.
Test mode start.
This pin is JTAG Test Mode Start. It is used to control the operation of the JTAG test.</td></tr>
<tr><td>E10</td><td>CD_VDD</td><td></td><td>Input Power</td><td>Power for the serial digital cable driver. Connect to 3.3V DC analog.</td></tr>
<tr><td>F1, F2, H1, H2, J1, J2, K1, K2, J3, K3</td><td>DIN[9:0]</td><td></td><td>Input</td><td>PARALLEL DATA BUS.
Signal levels are LVCMOS / LVTTL compatible.
<table><tr><td>20-bit mode
20BIT/$\overline{10BIT}$ = HIGH</td><td>DS2/Chroma data input in video mode
$\overline{656\_BYPASS}$ = HIGH
ASI = LOW
Data input in data through mode
$\overline{656\_BYPASS}$ = LOW
ASI = LOW
Not Used in ASI mode
$\overline{656\_BYPASS}$ = LOW
ASI = HIGH</td></tr><tr><td>10-bit mode
20BIT/$\overline{10BIT}$ = LOW</td><td>High impedance.</td></tr></table></td></tr>
<tr><td>F3</td><td>DETECT_TRS</td><td></td><td>Input</td><td>CONTROL SIGNAL INPUT.
Signal levels are LVCMOS / LVTTL compatible.
Used to select external HVF timing mode or TRS extraction timing mode.
When DETECT_TRS is LOW, the device extracts all internal timing from the supplied H:V:F or CEA-861 timing signals, dependent on the status of the 861_EN pin.
When DETECT_TRS is HIGH, the device extracts all internal timing from TRS signals embedded in the supplied video stream.</td></tr>
</table>

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
F8	TDO		Output	COMMUNICATION SIGNAL OUTPUT. Signal levels are LVCMOS/LVTTL compatible. Dedicated JTAG pin. JTAG Test Data Output. This pin is used to shift results from the device.
F10	RSET		Input	An external 1% resistor connected to this input is used to set the SDO/$\overline{\text{SDO}}$ output signal amplitude.
G1, H10	IO_VDD		Input Power	Power connection for digital I/O. Connect to 3.3V or 1.8V DC digital.
G2, H9	IO_GND		Input Power	Ground connection for digital I/O. Connect to digital GND.
G3	861_EN		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Used to select external CEA-861 timing mode. When DETECT_TRS is LOW and 861_EN is LOW, the device extracts all internal timing from the supplied H:V:F timing signals. When DETECT_TRS is LOW and 861_EN is HIGH, the device extracts all internal timing from the supplied HSYNC, VSYNC, DE timing signals. When DETECT_TRS is HIGH, the device extracts all internal timing from TRS signals embedded in the supplied video stream.
G4	20BIT/$\overline{\text{10BIT}}$		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. Used to select the input bus width.
G5	ASI		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable/disable the ASI data transmission. When ASI is set HIGH and $\overline{\text{656\_BYPASS}}$ is set LOW, the device carries out ASI word alignment, I/O processing and transmission. When $\overline{\text{656\_BYPASS}}$ and ASI are both set LOW, the device operates in data-through mode.
G6	$\overline{\text{656\_BYPASS}}$		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. Used to enable / disable all forms of encoding / decoding, scrambling and EDH insertion. When set LOW, the device operates in data through mode (ASI= LOW), or in ASI mode (ASI = HIGH). No video data scrambling takes place and none of the I/O processing features of the device are available when $\overline{\text{656\_BYPASS}}$ is set LOW. When set HIGH, the device carries out video data scrambling and I/O processing.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
G7	PROC_EN		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable the I/O processing features. When PROC_EN is HIGH, the I/O processing features of the device are enabled. When PROC_EN is LOW, the I/O processing features of the device are disabled. Only applicable in video mode.
G8	$\overline{\text{RESET}}$		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to reset the internal operating conditions to default settings.
H3	$\overline{\text{ANC\_BLANK}}$		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. When $\overline{\text{ANC\_BLANK}}$ is LOW, the Luma and Chroma input data is set to the appropriate blanking levels during the H and V blanking intervals. When $\overline{\text{ANC\_BLANK}}$ is HIGH, the Luma and Chroma data pass through the device unaltered. Only applicable in video mode.
H4	LOCKED		Output	STATUS SIGNAL OUTPUT. Signal levels are LVCMOS / LVTTL compatible. PLL lock indication. HIGH indicates PLL is locked. LOW indicates PLL is not locked.
H5	GRP2_EN		Input	Enable Input for audio channels 5-8. Set HIGH to enable.
H6	GRP1_EN		Input	Enable Input for audio channels 1-4. Set HIGH to enable.
H7	AUDIO_INT		Output	STATUS SIGNAL OUTPUT. Signal levels are LVCMOS / LVTTL compatible. Summary Interrupt from Audio Processing. This signal is set HIGH by the device to indicate a problem with the audio processing, which requires the Host processor to interrogate the interrupt status registers. IO_VDD = 3.3V Drive Strength = 8mA IO_VDD = 1.8V Drive Strength = 4mA **Note**: By default, out of reset, the AUDIO_INT pin outputs the HD_AUDIO_CLOCK, rather than the audio interrupt signal. In order to output the interrupt flags from the audio core as intended, the user must write 0001h to register 0232h.
J4	AIN5/6		Input	Serial Audio Input; Channels 5 and 6.
J5	WCLK2		Input	48kHz Word clock for Channels 5-8.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
J6	AIN1/2		Input	Serial Audio Input; Channels 1 and 2.
J7	WCLK1		Input	48kHz Word clock for Channels 1-4.
J8	TCK		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. JTAG Serial Data Clock Signal. This pin is the JTAG clock.
J9	SDOUT		Output	COMMUNICATION SIGNAL OUTPUT. Signal levels are LVCMOS / LVTTL compatible. Serial Data Output. This pin operates as the host interface serial output, used to read status and configuration information from the internal registers of the device. IO_VDD = 3.3V Drive Strength = 12mA IO_VDD = 1.8V Drive Strength = 4mA
J10	SCLK		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Serial data clock signal. SCLK operates as the host interface burst clock, SCLK. Command and data read/write words are clocked into the device synchronously with this clock. **Note**: If the host interface is not being used, tie this pin HIGH.
K4	AIN7/8		Input	Serial Audio Input; Channels 7 and 8.
K5	ACLK2		Input	64 x WCLK for Channels 5-8.
K6	AIN3/4		Input	Serial Audio Input; Channels 3 and 4.
K7	ACLK1		Input	64 x WCLK for Channels 1-4.
K9	$\overline{CS}$		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Chip select. $\overline{CS}$ operates as the host interface Chip Select, and is active LOW.
K10	SDIN		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Serial data in. This pin is used to write address and configuration data words into the device.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Digital Core (CORE_VDD)	-0.3V to +1.5V
Supply Voltage, Digital I/O (IO_VDD)	-0.3V to +3.6V
Supply Voltage, Analog 1.2V (PLL_VDD, VCO_VDD)	-0.3V to +1.5V
Supply Voltage, Analog 3.3V (CD_VDD, AVDD)	-0.3V to +3.6V
Input Voltage Range (RSET)	-0.3V to (CD_VDD + 0.3)V
Input Voltage Range (VBG)	-0.3V to (AVDD + 0.3)V
Input Voltage Range (LF)	-0.3V to (PLL_VDD + 0.3)V
Input Voltage Range (digital inputs)	-2.0V to +5.25V
Ambient Operating Temperature (T_A)	$-40°C \leq T_A \leq 95°C$
Storage Temperature (T_{STG})	$-40°C \leq T_{STG} \leq 125°C$
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	2kV

Notes:

Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Operating Temperature Range, Ambient	T_A	–	-20	–	85	°C	–
Supply Voltage, Digital Core	CORE_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V	–
		3.3V mode	3.13	3.3	3.47	V	–
Supply Voltage, PLL	PLL_VDD	–	1.14	1.2	1.26	V	–

Table 2-2: Recommended Operating Conditions (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage, VCO	VCO_VDD	–	–	0.7	–	V	1
Supply Voltage, Analog	AVDD	–	3.13	3.3	3.47	V	–
Supply Voltage, CD	CD_VDD	–	3.13	3.3	3.47	V	–

Notes:

1. This is 0.7V rather than 1.2V because there is a voltage drop across an external 105Ω resistor.

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

Guaranteed over recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
+1.2V Supply Current	I_{1V2}	10-bit Full HD	–	135	200	mA	–
		20-bit Full HD	–	135	200	mA	–
		10/20-bit HD	–	100	160	mA	–
		10/20-bit SD	–	75	120	mA	–
		ASI	–	75	120	mA	–
+1.8V Supply Current	I_{1V8}	10-bit Full HD	–	15	30	mA	–
		20-bit Full HD	–	15	32	mA	–
		10/20-bit HD	–	15	32	mA	–
		10/20-bit SD	–	3	10	mA	–
		ASI	–	3	10	mA	–
+3.3V Supply Current	I_{3V3}	10-bit Full HD	–	90	110	mA	–
		20-bit Full HD	–	90	110	mA	–
		10/20-bit HD	–	90	110	mA	–
		10/20-bit SD	–	70	90	mA	–
		ASI	–	70	90	mA	–
Total Device Power (IO_VDD = 1.8V)	P_{1D8}	10-bit Full HD	–	400	560	mW	–
		20-bit Full HD	–	400	560	mW	–
		10/20-bit HD	–	350	510	mW	–
		10/20-bit SD	–	300	450	mW	–
		ASI	–	300	450	mW	–
		Reset	–	200	–	mW	–
		Standby	–	110	150	mW	–

Table 2-3: DC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Total Device Power (IO_VDD = 3.3V)	P_{3D3}	10-bit Full HD	–	430	600	mW	–
		20-bit Full HD	–	450	610	mW	–
		10/20-bit HD	–	420	550	mW	–
		10/20-bit SD	–	320	450	mW	–
		ASI	–	320	450	mW	–
		Reset	–	230	–	mW	–
		Standby	–	110	150	mW	–
Digital I/O							
Input Logic LOW	V_{IL}	3.3V or 1.8V operation	IO_GND - 0.3	–	0.3 x IO_VDD	V	–
Input Logic HIGH	V_{IH}	3.3V or 1.8V operation	0.7 x IO_VDD	–	IO_VDD + 0.3	V	–
Output Logic LOW	V_{OL}	IOL=5mA, 1.8V operation	–	–	0.2	V	–
		IOL=8mA, 3.3V operation	–	–	0.4	V	–
Output Logic HIGH	V_{OH}	IOL=5mA, 1.8V operation	1.4	–	–	V	–
		IOL=8mA, 3.3V operation	2.4	–	–	V	–
Serial Output							
Serial Output Common Mode Voltage	V_{CMOUT}	75Ω load, RSET = 750Ω SD and HD mode	–	CD_VDD - $\Delta V_{SDO}/2$	–	V	–

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

Guaranteed over recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
Reset Pulse Width	t_{reset}	–	1	–	–	ms	–
Device Latency							
Full HD Bypass Mode		PCLK = 148.5MHz	–	54	–	PCLK	–
Full HD Video Mode		PCLK = 148.5MHz (no audio)	–	95	–	PCLK	–
Full HD Video Mode		PCLK = 148.5MHz (with audio)	–	1106	–	PCLK	–
HD Bypass Mode		PCLK = 74.25MHz	–	54	–	PCLK	–
HD Video Mode		PCLK = 74.25MHz (no audio)	–	95	–	PCLK	–
HD Video Mode		PCLK = 74.25MHz (with audio)	–	1106	–	PCLK	–
SD Bypass Mode		PCLK = 27MHz	–	54	–	PCLK	–
SD Video Mode		PCLK = 27MHz (no audio)	–	112			
SD Video Mode		PCLK = 27MHz (with audio)	–	638	–	PCLK	–
ASI Mode		PCLK = 27MHz	–	52	–	PCLK	–
Parallel Input							
Parallel Clock Frequency	f_{PCLK}	–	13.5	–	148.5	MHz	–
Parallel Clock Duty Cycle	DC_{PCLK}	–	40	–	60	%	–
Input Data Setup Time	t_{su}	50% levels; 3.3V or 1.8V operation	1.2	–	–	ns	1
Input Data Hold Time	t_{ih}		0.8	–	–	ns	1
Serial Audio Data Input							
Input Data Set-up Time	t_{su}	50% levels; 3.3V or 1.8V operation	74	–	–	ns	–
Input Data Hold Time	t_{ih}		74	–	–	ns	–
Serial Digital Output							
Serial Output Data Rate	DR_{SDO}	–	–	2.97	–	Gb/s	–
		–	–	2.97/1.001	–	Gb/s	–
		–	–	1.485	–	Gb/s	–
		–	–	1.485/1.001	–	Gb/s	–
		–	–	270	–	Mb/s	–

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Output Swing	V_{SDD}	RSET = 750Ω 75Ω load	750	800	850	mVp-p	2
Serial Output Rise/Fall Time 20% ~ 80%	trf_{SDO}	HD mode	–	120	135	ps	–
	trf_{SDO}	SD mode	400	660	800	ps	–
Mismatch in rise/fall time	$\Delta t_r, \Delta t_f$	–	–	–	35	ps	–
Duty Cycle Distortion	–	–	–	–	5	%	2
Overshoot	–	HD mode	–	5	10	%	2
	–	SD mode	–	3	8	%	2
Output Return Loss	ORL	1.485GHz - 2.97GHz	–	-12	–	dB	3
		5MHz - 1.485GHz	–	-18	–	dB	3
Serial Output Intrinsic Jitter	t_{OJ}	Pseudorandom and Colour Bars HD signal	–	40	68	ps	4, 5
	t_{OJ}	Pseudorandom and Colour Bars SD signal	–	50	95	ps	4, 5
Serial Output Intrinsic Jitter	t_{OJ}	Pseudorandom and Colour Bars SD signal	–	200	400	ps	6
GSPI							
GSPI Input Clock Frequency	f_{SCLK}	50% levels 3.3V or 1.8V operation	–	–	80	MHz	–
GSPI Input Clock Duty Cycle	DC_{SCLK}		40	50	60	%	–
GSPI Input Data Setup Time	–		1.5	–	–	ns	–
GSPI Input Data Hold Time	–		1.5	–	–	ns	–
GSPI Output Data Hold Time	–	15pF load	1.5	–	–	ns	–
$\overline{CS}$ low before SCLK rising edge	t_0	50% levels 3.3V or 1.8V operation	1.5	–	–	ns	7
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle	t_4	50% levels 3.3V or 1.8V operation	PCLK (MHz) / ns: unlocked 445; 13.5 74.2; 27.0 37.1; 74.25 13.5; 148.5 6.7	–	–	ns	7

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Conditions	Min		Typ	Max	Units	Notes
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle	t_5	50% levels 3.3V or 1.8V operation	PCLK (MHz)	ns	–	–	ns	7
			unlocked	1187				
			13.5	297				
			27.0	148.4				
			74.25	53.9				
			148.5	27				
$\overline{CS}$ high after SCLK rising edge	t_7	50% levels 3.3V or 1.8V operation	PCLK (MHz)	ns	–	–	ns	7
			unlocked	445				
			13.5	74.2				
			27.0	37.1				
			74.25	13.5				
			148.5	6.7				

Notes:

1. Input setup and hold time is dependent on the rise and fall time on the parallel input. Parallel clock and data with rise time or fall time greater than 500ps require larger setup and hold times.
2. Single Ended into 75Ω external load.
3. ORL depends on board design.
4. Alignment Jitter = measured from 100kHz to serial data rate/10.
5. This is the maximum jitter for a BER 10^{-12}. The equivalent jitter value as per RP184 is 40ps max.
6. Alignment Jitter = measured from 1kHz to 27MHz.
7. For GSPI timing parameters, refer to Figure 4-52 and Figure 4-53 in Section 4.14.3, as appropriate.

3. Input/Output Circuits

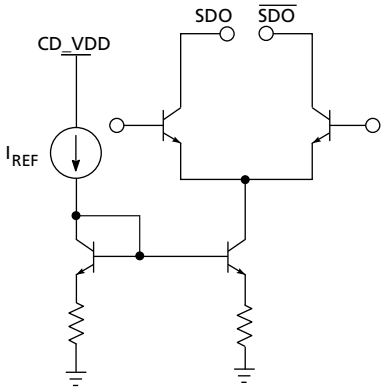


Figure 3-1: Differential Output Stage (SDO/SDO)

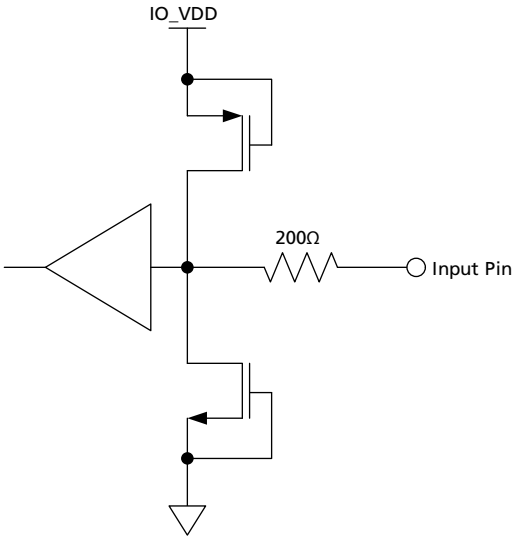


Figure 3-2: Digital Input Pin (20BIT/10BIT, ANC_BLANK, DETECT_TRS, ASI, RATE_SEL0, 656_BYPASS, RATE_SEL1, 861_EN, F/DE, H/HSYNC, PCLK, V/VSYNC)

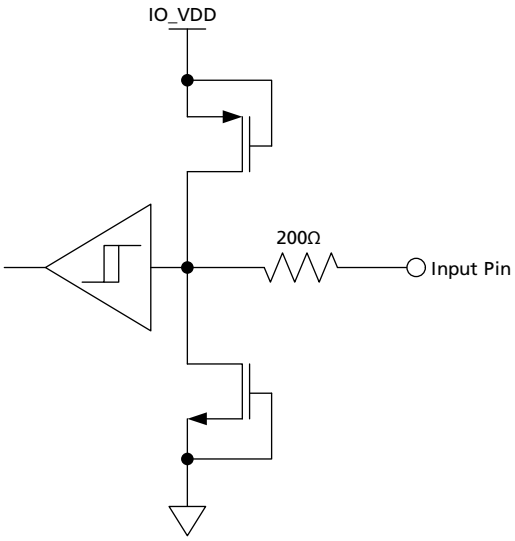


Figure 3-3: Digital Input Pin with Schmitt Trigger ($\overline{\text{RESET}}$)

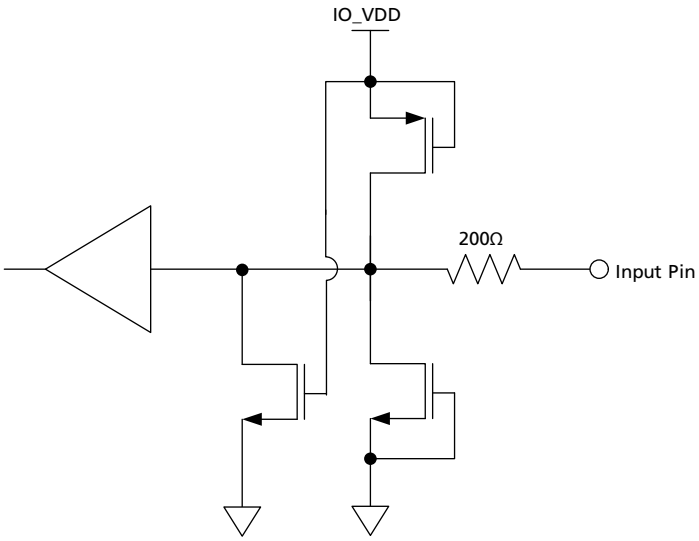


Figure 3-4: Digital Input Pin with weak pull-down - maximum pull-down current <110mA (STANDBY, SCLK, SDIN, TCK, TDI)

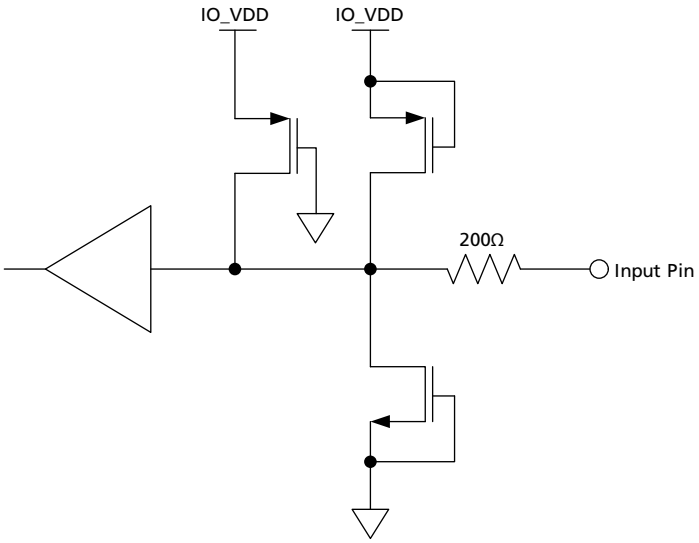


Figure 3-5: Digital Input Pin with weak pull-up - maximum pull-up current <110mA (ACLK1, ACLK2, AIN7/8, AIN5/6, AIN3/4, AIN1/2, $\overline{CS}$, GRP1_EN, GRP2_EN, PROC_EN, SDO_EN, TMS, WCLK1, WCLK2)

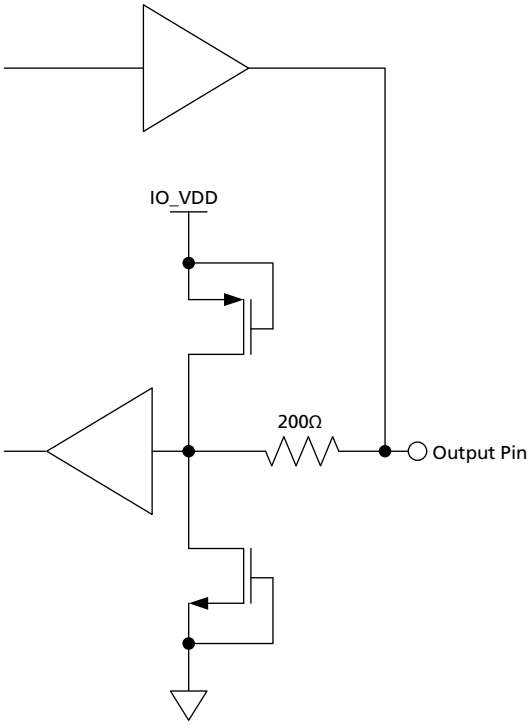


Figure 3-6: Bidirectional Digital Input/Output Pin with programmable drive strength.

These pins in Figure 3-6 are configured to input at all times except in test mode. (DIN0, DIN2, DIN3, DIN4, DIN5, DIN6, DIN7, DIN8, DIN9, DIN10, DIN11, DIN12, DIN13, DIN14, DIN15, DIN16, DIN17, DIN18, DIN19, DIN1)

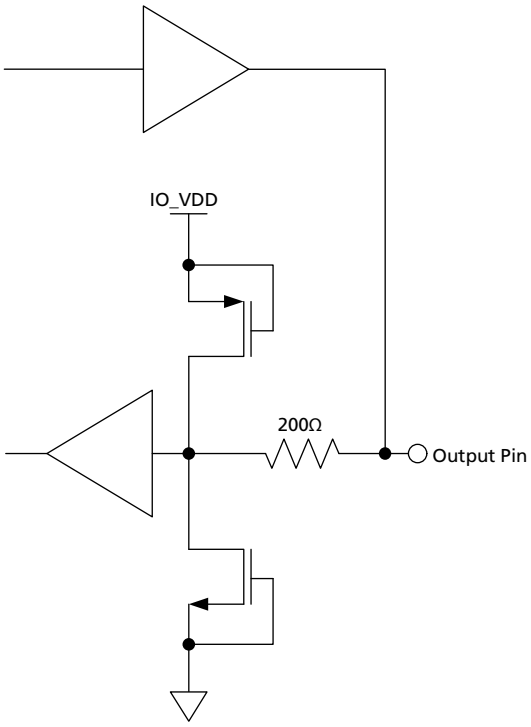


Figure 3-7: Bidirectional Digital Input/Output Pin with programmable drive strength.

These pins in Figure 3-7 are configured to output at all times except in reset mode. (LOCKED, AUDIO_INT, SDOUT, TDO)

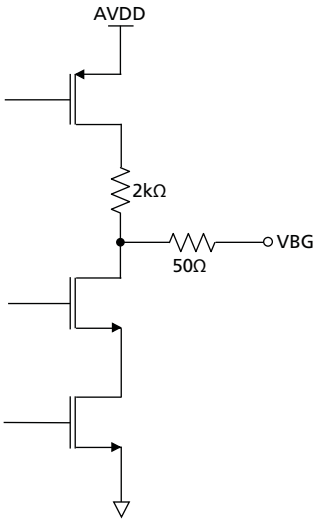


Figure 3-8: VBG

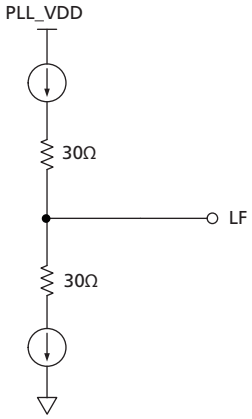


Figure 3-9: Loop Filter

4. Detailed Description

4.1 Functional Overview

The GV7600 is a Multi-Rate Aviia Transmitter with an Integrated Cable Driver and Embedded Audio Multiplexer. It provides a complete transmit solution for standard definition and high definition video, up to 1080 lines 50/60Hz progressive.

The device has three basic modes of operation that must be set through external device pins: Video mode, ASI mode, and Data-Through mode.

In Video mode, the device accepts 10-bit multiplexed or 20-bit demultiplexed video data, compliant to ITU-R BT.656 and BT.1120. By default, the device's additional processing features, including audio embedding, are enabled in this mode.

In ASI mode, the GV7600 accepts an 8-bit parallel IEC 13818-1 compliant transport stream on DIN[17:10]. The serial output data stream is 8b/10b encoded with stuffing characters added.

Data-Through mode allows for the serializing of data not conforming to standard video or ASI streams. No additional processing is done in this mode.

In addition, the device may be put into Standby, to reduce power consumption.

The serial digital output features a high-impedance mode and adjustable signal swing. The output slew rate is automatically set by the RATE_SEL0 and RATE_SEL1 pin setting.

The GV7600 provides several data processing functions; including generic ancillary data insertion, and Error Detection & Handling (EDH) data packet generation and insertion, automatic video standards detection, and TRS, CRC, checksum, and line number calculation and insertion. These features are all enabled/disabled collectively using the external I/O processing pin, but may be individually disabled via internal registers accessible through the GSPI host interface.

Finally, the GV7600 has a JTAG interface for boundary scan test implementations.

4.2 Parallel Video Data Inputs DIN[9:0] & DIN[19:10]

Data signal inputs enter the device on the rising edge of PCLK, as shown in Figure 4-1.

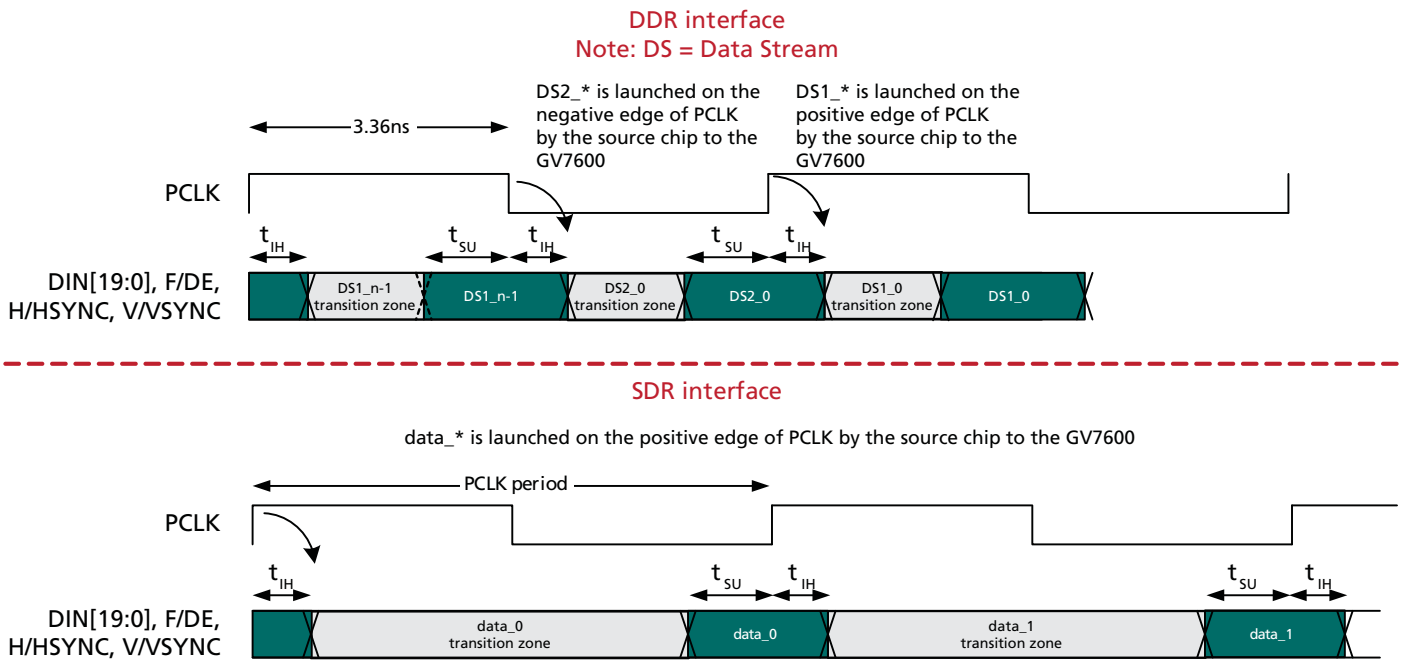


Figure 4-1: GV7600 Video and Host Interface Timing Diagrams

Table 4-1: GV7600 Parallel Input AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input data set-up time	t_{SU}	50% levels; 1.8V operation	1.2	–	–	ns
Input data hold time	t_{IH}		0.8	–	–	ns
Input data set-up time	t_{SU}	50% levels; 3.3V operation	1.3	–	–	ns
Input data hold time	t_{IH}		0.8	–	–	ns

Table 4-2: GV7600 Input Video Data Format Selections

Input Data Format	Pin/Register Bit Settings					DIN[9:0]	DIN[19:10]
	20BIT /10BIT	RATE _SEL0	RATE _SEL1	656_ BYPASS	ASI		
20-bit demultiplexed Full HD	HIGH	LOW	HIGH	HIGH	LOW	Data Stream 2	Data Stream 1
20-bit data Input Full HD	HIGH	LOW	HIGH	LOW	LOW	DATA	DATA
20-bit demultiplexed HD format	HIGH	LOW	LOW	HIGH	LOW	Chroma	Luma
20-bit data Input HD format	HIGH	LOW	LOW	LOW	LOW	DATA	DATA
20-bit demultiplexed SD format	HIGH	HIGH	X	HIGH	LOW	Chroma	Luma
20-bit data input SD format	HIGH	HIGH	X	LOW	LOW	DATA	DATA
10-bit multiplexed Full HD DDR format	LOW	LOW	HIGH	HIGH	LOW	High Impedance	Data Stream 1 / Data Stream 2
10-bit multiplexed HD format	LOW	LOW	LOW	HIGH	LOW	High Impedance	Luma/Chroma
10-bit data input HD format	LOW	LOW	LOW	LOW	LOW	High Impedance	DATA
10-bit multiplexed SD format	LOW	HIGH	X	HIGH	LOW	High Impedance	Luma/Chroma
10-bit multiplexed SD format	LOW	HIGH	X	LOW	LOW	High Impedance	DATA
10-bit ASI input	LOW	HIGH	X	LOW	HIGH	High Impedance	ASI data

The GV7600 is a high performance serial digital video and audio transmitter. In order to optimize the output jitter performance across all operating conditions, input levels and overshoot at the parallel video data inputs of the device need to be controlled. In order to do this, source series termination resistors should be used to match the impedance of the PCB data trace line. IBIS models can be used to simulate the board effects and then optimize the output drive strength and the termination resistors to allow for the best transition (one that produces minimal overshoot). If this is not viable, Gennum recommends matching the source series resistance to the trace impedance, and then adjusting the output drive strength to the minimum value that gives zero errors.

The above also applies to the PCLK input line. HVF and the Audio inputs should also be well terminated, however due to the lower data rates and transition density it is not as critical.

4.2.1 Parallel Input In Video Mode

When the device is operating in video mode ($\overline{656\_BYPASS}$ = HIGH), data must be presented to the input bus in either multiplexed or demultiplexed form, depending on the setting of the 20BIT/$\overline{10BIT}$ pin.

When operating in 20-bit mode (20BIT/$\overline{10BIT}$ = HIGH), the input data format must be word aligned, demultiplexed Luma and Chroma data (SD or HD), or word aligned demultiplexed Data Stream 1 (DS1) and Data Stream 2 (DS2) data (full HD).

When operating in 10-bit mode (20BIT/$\overline{10BIT}$ = LOW), the input data format must be word aligned, multiplexed Luma and Chroma data (SD, HD and full HD). In this mode, the data must be presented on the DIN[19:10] pins. The DIN[9:0] inputs are ignored.

In full HD 10-bit mode, the device operates in DDR mode. That is, the input data is sampled on both the rising and falling edges of the PCLK. In full HD mode, DS2 words precede DS1 words. The DS2 words are sampled on the rising edge of the input PCLK, and the DS1 words are sampled on the following falling edge. H, V and F timing pulses, if used, are sampled on the rising edge of PCLK.

4.2.1.1 Standard Definition Video Input Formats

ITU-R BT.656 (formally CCIR-656) defines an 8-bit, 10-bit or 12-bit parallel interface for transmitting 4:2:2 YCbCr digital video. To reduce the number of wires required for the interface, timing codes are embedded in the video stream to provide information traditionally transmitted by dedicated HSYNC, VSYNC, and BLANK signals. Ancillary digital data such as audio and closed captioning may be transmitted during blanking intervals (see Figure 4-2 and Figure 4-4). Figure 4-3 shows the multiplexed 10-bit 4:2:2 YCbCr data for 525 line video at 60Hz. Figure 4-5 shows the multiplexed 10-bit 4:2:2 YCbCr data for 625 line video at 50Hz. The start of active video and the end of active video are marked by the SAV and EAV codes, respectively. The values of these codes are reserved for this purpose and should not occur elsewhere in the video raster. F, V, H timing information is stored in the 10-bit XYZ word as follows:

- Bit 8 - (F-bit) 0 for field one; and 1 for field two
- Bit 7 - (V-bit) 1 in vertical blanking interval; and 0 during active video lines
- Bit 6 - (H-bit) 1 indicates the EAV sequence; and 0 indicates the SAV sequence

The two LSB's of the XYZ word are set to zero for compatibility with 8-bit systems.

Table 4-3: 525/60Hz Format

Line Number	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-20	0	1	1	0
21-263	0	0	1	0
264-265	0	1	1	0
266-282	1	1	1	0
283-525	1	0	1	0

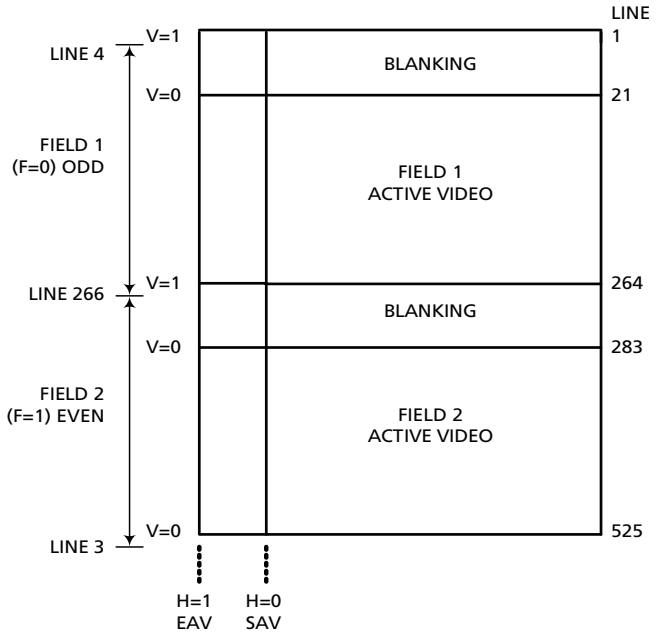


Figure 4-2: Data transmitting with blanking, 525/60Hz

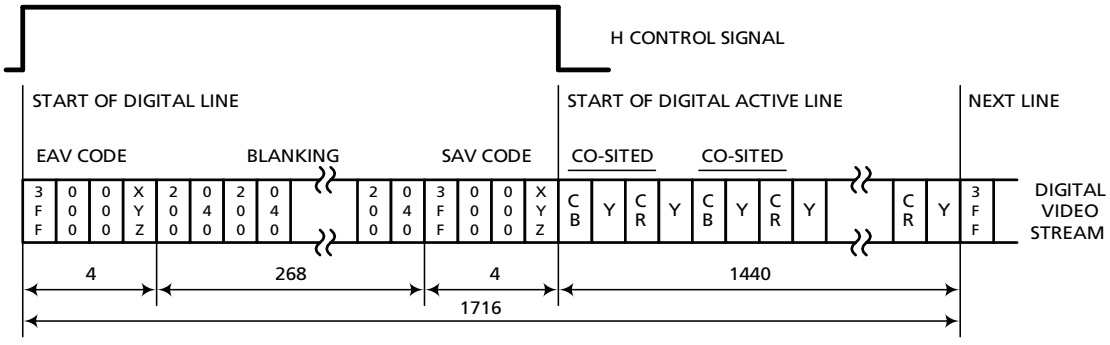


Figure 4-3: Multiplexing 10-bit 4:2:2 YCbCr data for 525 lines at 60Hz

Table 4-4: 625/50Hz Format

Line Number	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
336-623	1	0	1	0
624-625	1	1	1	0

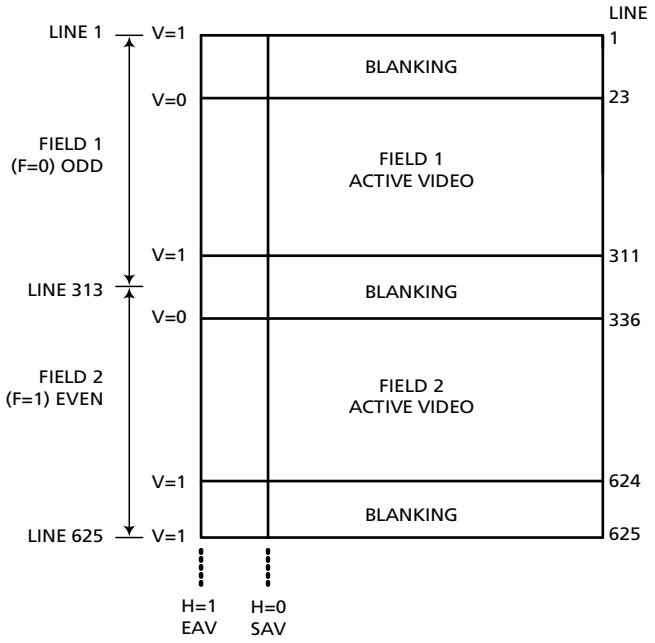


Figure 4-4: Data transmitting with blanking, 625/50Hz

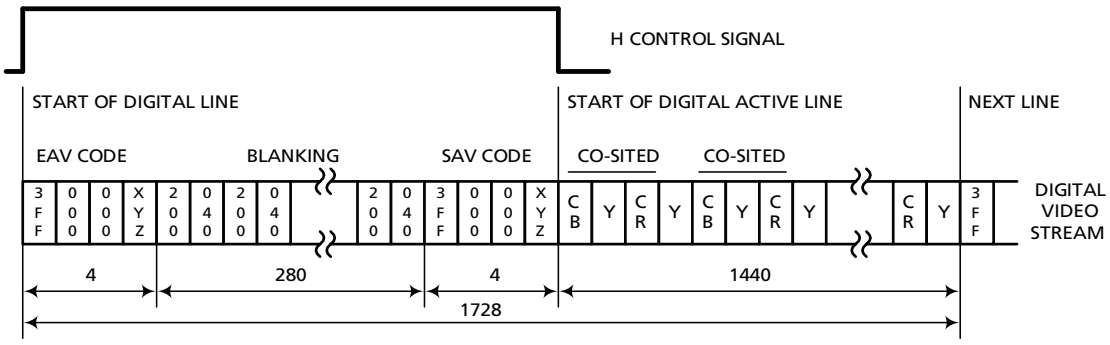


Figure 4-5: Multiplexing 10-bit 4:2:2 YCbCr data for 625 lines at 50Hz

4.2.1.2 High Definition Video Input Formats

ITU-R BT.1120 describes the serial and parallel format for 1080-line interlaced and progressive digital video. As with ITU-R BT.656, the field/frame blanking period (V), the line blanking period (H), and the field identification (F), are embedded as digital timing codes (TRS) within the video. Data is transmitted over two 10-bit buses, one for luma (Y') and one for colour difference ($C'_BC'_R$), operating at a clock rate of 74.25MHz or 74.25/1.001 MHz. Prior to serialization, the two 10-bit buses are interleaved onto a single 10-bit bus following the pattern C'_B, Y', C'_R, Y', etc.

The following figures show horizontal and vertical timing for 1080-line interlaced systems.

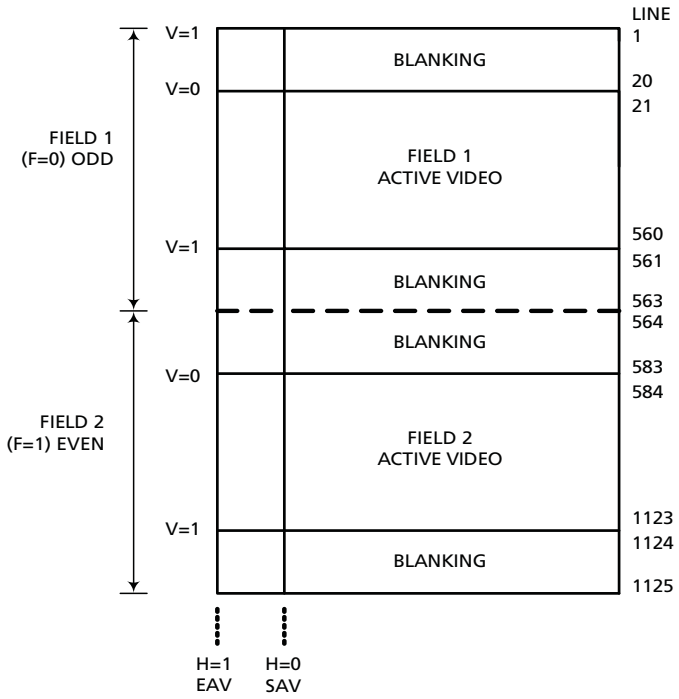


Figure 4-6: Field Timing Relationship for 1080-line Interlaced Systems

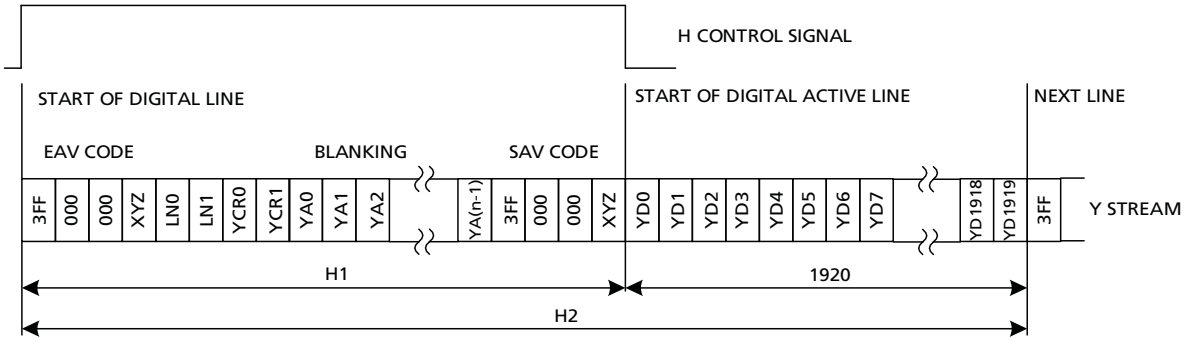


Figure 4-7: Luma Stream Over One Video Line - 1080i

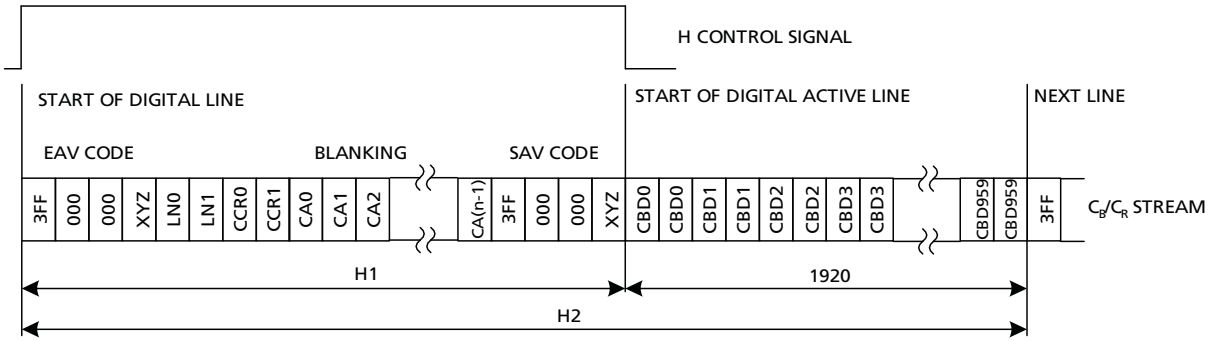


Figure 4-8: Chroma Stream Over One Video Line - 1080i

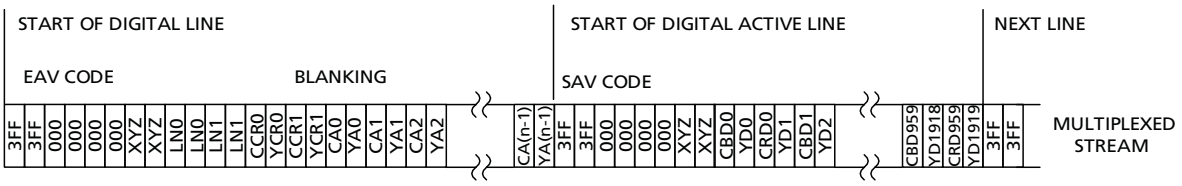


Figure 4-9: Multiplexed Luma and Chroma Over One Video Line - 1080i

Table 4-5: 1080-line Interlaced Horizontal Timing

Interlaced	60 or 60/1.001 Hz	50Hz
H1	280	720
H2	2200	2640

4.2.1.3 High Definition 1080p Input Formats

ITU-R BT.1120 also includes progressive scan formats with 1080 active lines, with $Y'C'_BC'_R$ 4:2:2 sampling at pixel rates of 74.25MHz or 74.25/1.001 MHz. The following diagrams show horizontal and vertical timing for 1080-line progressive systems.

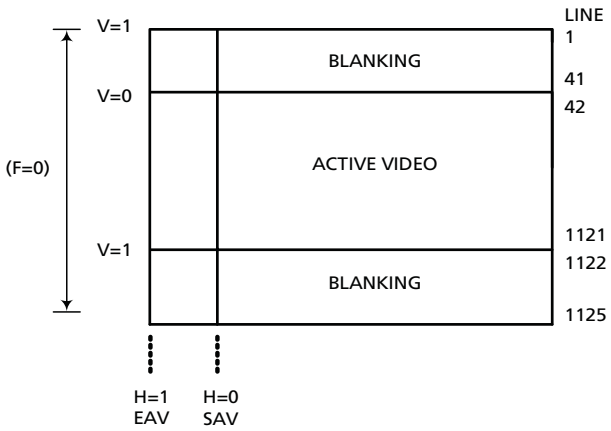


Figure 4-10: Frame Timing Relationship For 1080-line Progressive Systems

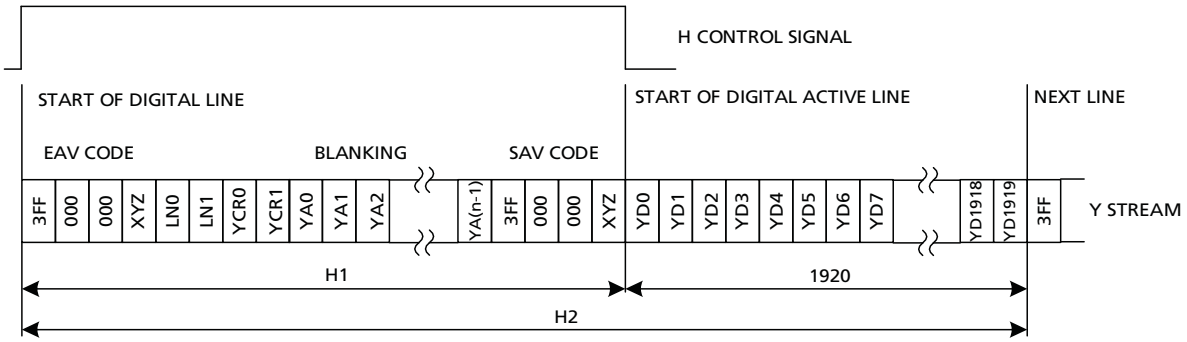


Figure 4-11: Luma Stream Over One Video Line - 1080p

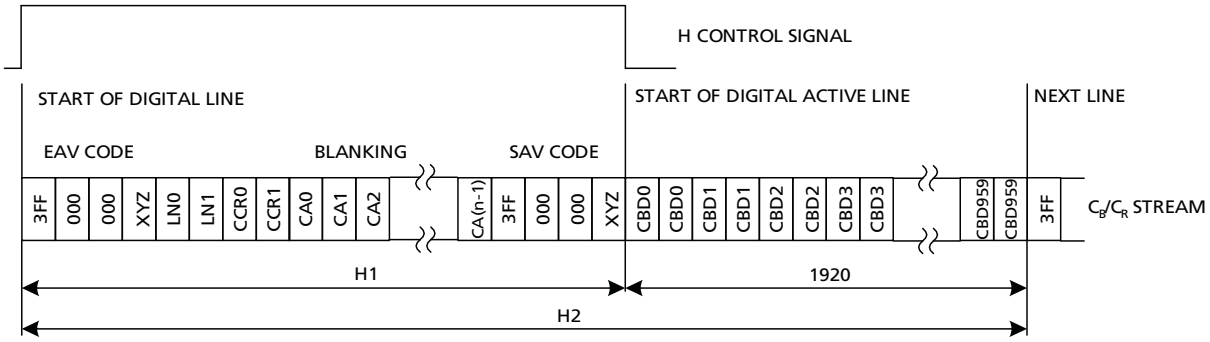


Figure 4-12: Chroma Stream Over One Video Line - 1080p

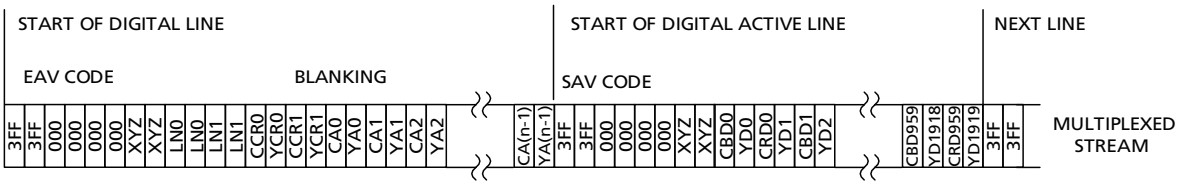


Figure 4-13: Multiplexed Luma and Chroma Over One Video Line - 1080p

Table 4-6: 1080-line Progressive Horizontal Timing

Progressive	30 or 30/1.001 Hz	25Hz	24 or 24/1.001 Hz
H1	280	720	830
H2	2200	2640	2750

4.2.1.4 High Definition 720p Input Formats

The Society of Motion Picture and Television Engineers (SMPTE) defines the standard for progressive scan 720-line HD image formats. SMPTE 296M-2001 specifies the representation for 720p digital $Y'C'_BC'_R$ 4:2:2 signals at pixel rates of 74.25MHz or 74.25/1.001 MHz.

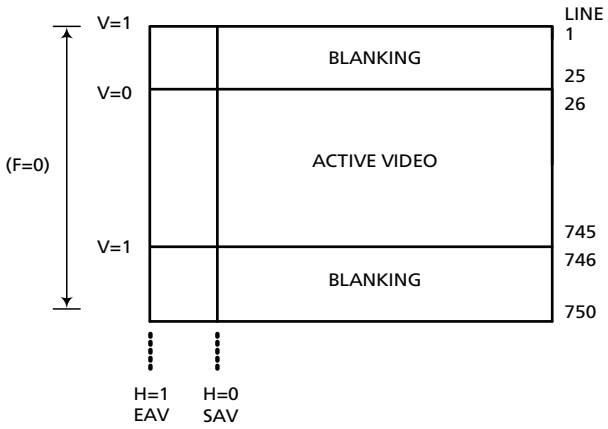


Figure 4-14: 720p Digital Vertical Timing

The frame rate determines the horizontal timing, which is shown in Table 4-7.

Table 4-7: 720p Horizontal Timing

Frame Rate	H = 1 Sample Number	H = 0 Sample Number
24 or 24/1.001	1283	4124
25	1283	3959
30 or 30/1.001	1283	3299
50	1283	1979
60 or 60/1.001	1283	1649

4.2.1.5 Full HD Input Formats

High definition input formats that require the Aviia serial data rate to operate at 2.97Gb/s are defined as Full HD formats. These formats are generally 1080-line based, operating at 50 or 60Hz progressive frame rate. However, the sampling structure and bit-depth of HD formats may also increase the payload rate at the digital input of the GV7600. There are also 720-line Full HD formats with 4:4:4 sampling.

The GV7600 can support the progressive scan Full HD formats shown in Table 4-8.

Table 4-8: Full HD 1080-line and 720-line Progressive Image Formats

Active Image Format	Total Pixels x Lines	Sampling Structure	Pixel Depth	Frame Rate (Hz)
1920 x 1080	2640 x 1125	4:2:2 ($Y'C'_BC'_R$)	8 or 10-bit	50
	2200 x 1125			60 or 60/1.001
	2750 x 1125	4:4:4 (R'G'B' or $Y'C'_BC'_R$)	8 or 10-bit	24 or 24/1.001
	2640 x 1125			25
	2200 x 1125			30 or 30/1.001
	2750 x 1125	4:4:4 (R'G'B' or $Y'C'_BC'_R$)	12-bit	24 or 24/1.001
	2640 x 1125			25
	2200 x 1125			30 or 30/1.001
	2750 x 1125	4:2:2 ($Y'C'_BC'_R$)	12-bit	24 or 24/1.001
	2640 x 1125			25
	2200 x 1125			30 or 30/1.001
1280 x 720	1980 x 750	4:2:2 ($Y'C'_BC'_R$)	8 or 10-bit	100
	1650 x750			120 or 120/1.001
	4125 x 750	4:4:4 (R'G'B' or $Y'C'_BC'_R$)	8 or 10-bit	24 or 24/1.001
	3960 x 750			25
	3300 x 750			30 or 30/1.001
	1980 x 750			50
	1650 x 750			60 or 60/1.001

Full HD formats must be input to the GV7600 using a 20-bit input bus format at a clock rate of 148.5 MHz. The 20-bit input format consists of two 10-bit data streams, DS1 and DS2. The following diagrams show how the Full HD image formats should be multiplexed into DS1 and DS2, at the input of the GV7600.

The GV7600 also supports a 10-bit DDR input mode, where DS1 and DS2 are word multiplexed.

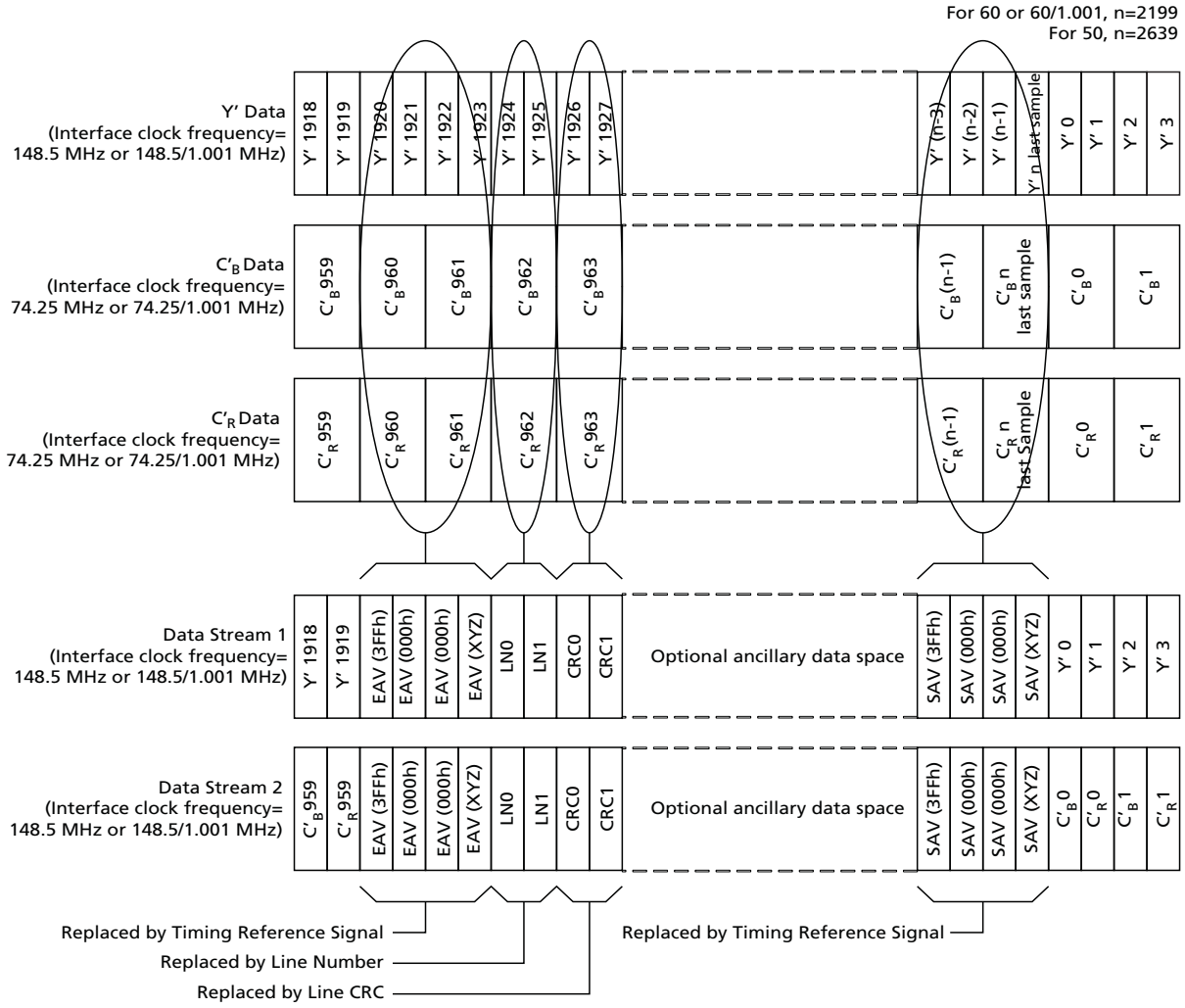


Figure 4-15: Aviia 20-bit Mapping Structure for 1920 x 1080 50/60Hz Progressive 4:2:0 & 4:2:2 (Y'C'$_B$C'$_R$) 8/10-bit Signals

Table 4-9: 1080p Y'C'$_B$C'$_R$ 4:2:0 & 4:2:2 10-bit Bit Structure Mapping

	Bit Number									
Data Stream	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DS1	Y'[9:0]									
DS2	C'$_B$C'$_R$[9:0]									

Note: For 8-bit systems, the data should be justified to the most significant bit (Y'9 and C'$_B$C'$_R$9), with the two least significant bits (Y'[1:0] and C'$_B$C'$_R$[1:0]) set to zero.

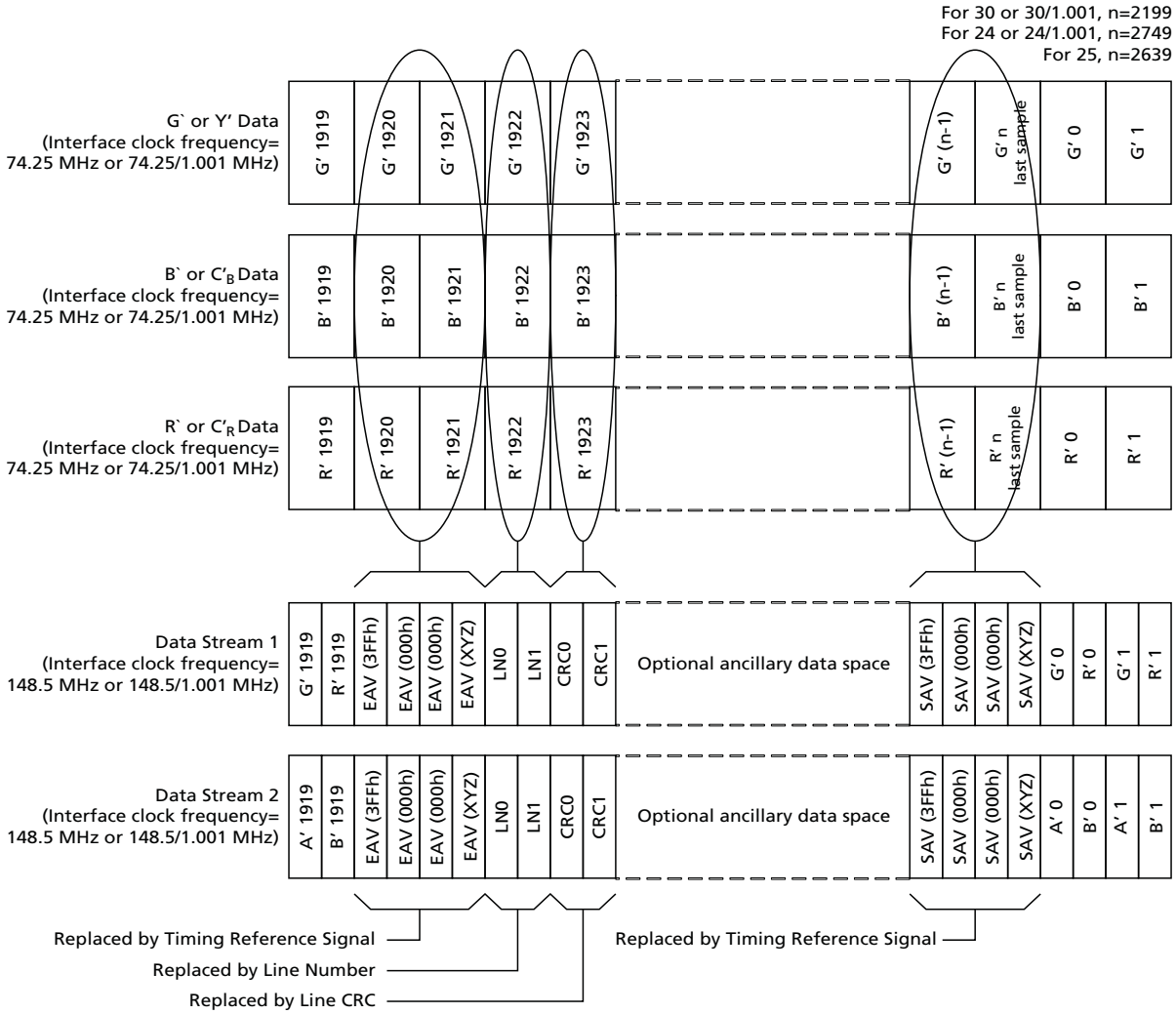


Figure 4-16: Aviia 20-bit Mapping Structure for 1920 x 1080 24/25/30Hz Progressive 4:4:4 (R'G'B') 8/10-bit Signals

Table 4-10: 1080p R'G'B' or Y'C'$_B$C'$_R$ 4:4:4 10-bit Bit Structure Mapping

	Bit Number									
Data Stream	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DS1 First Word	G'[9:0] or Y'[9:0]									
DS1 Second Word	R'[9:0] or C'$_R$[9:0]									
DS2 First Word	A'[9:0]									
DS2 Second Word	B'[9:0] or C'$_B$[9:0]									

Note 1: The 10-bit 'A' data in Figure 4-16 is used to pad DS2 and should be set to the value 040h.

Note 2: For 8-bit systems, the data should be justified to the most significant bit (R'/C'$_R$9, G'/Y'9 and B'/C'$_B$9), with the two least significant bits (R'/C'$_R$[1:0], G'/Y'[1:0] and B'/C'$_B$[1:0]) set to zero.

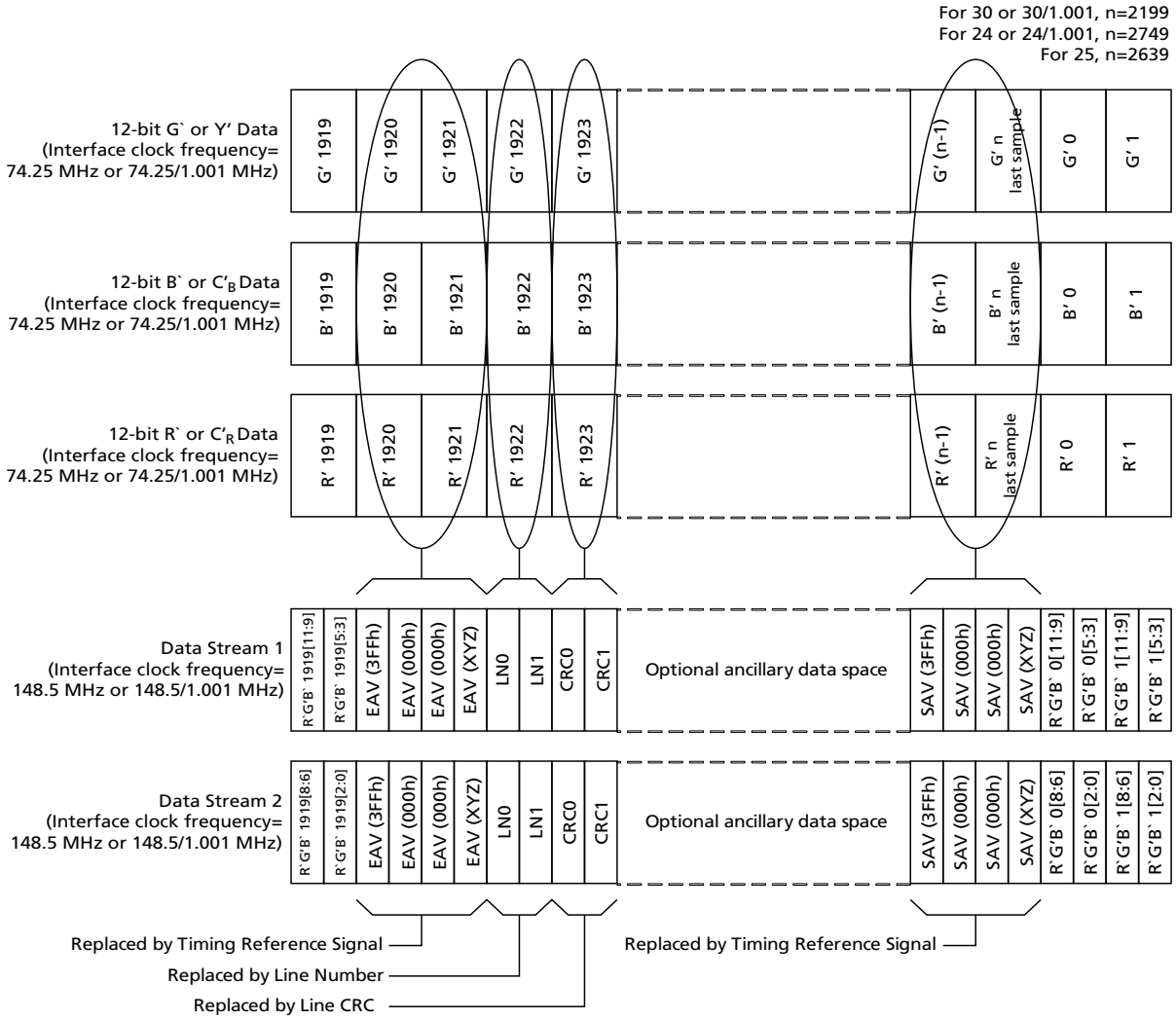


Figure 4-17: Aviia 20-bit Mapping Structure for 1920 x 1080 24/25/30Hz Progressive 4:4:4 (R'G'B' or Y'C'$_B$C'$_R$) 12-bit Signals

Table 4-11: 1080p R'G'B' or Y'C'$_B$C'$_R$ 4:4:4 12-bit Bit Structure Mapping

	Bit Number									
Data Stream	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DS1 First Word	$\overline{B8}$	R'[11:9] or C'$_R$[11:9]			G'[11:9] or Y'[11:9]			B'[11:9] or C'$_B$[11:9]		
DS1 Second Word	$\overline{B8}$	R'[5:3] or C'$_R$[5:3]			G'[5:3] or Y'[5:3]			B'[5:3] or C'$_B$[5:3]		
DS2 First Word	$\overline{B8}$	R'[8:6] or C'$_R$[8:6]			G'[8:6] or Y'[8:6]			B'[8:6] or C'$_B$[8:6]		
DS2 Second Word	$\overline{B8}$	R'[2:0] or C'$_R$[2:0]			G'[2:0] or Y'[2:0]			B'[2:0] or C'$_B$[2:0]		

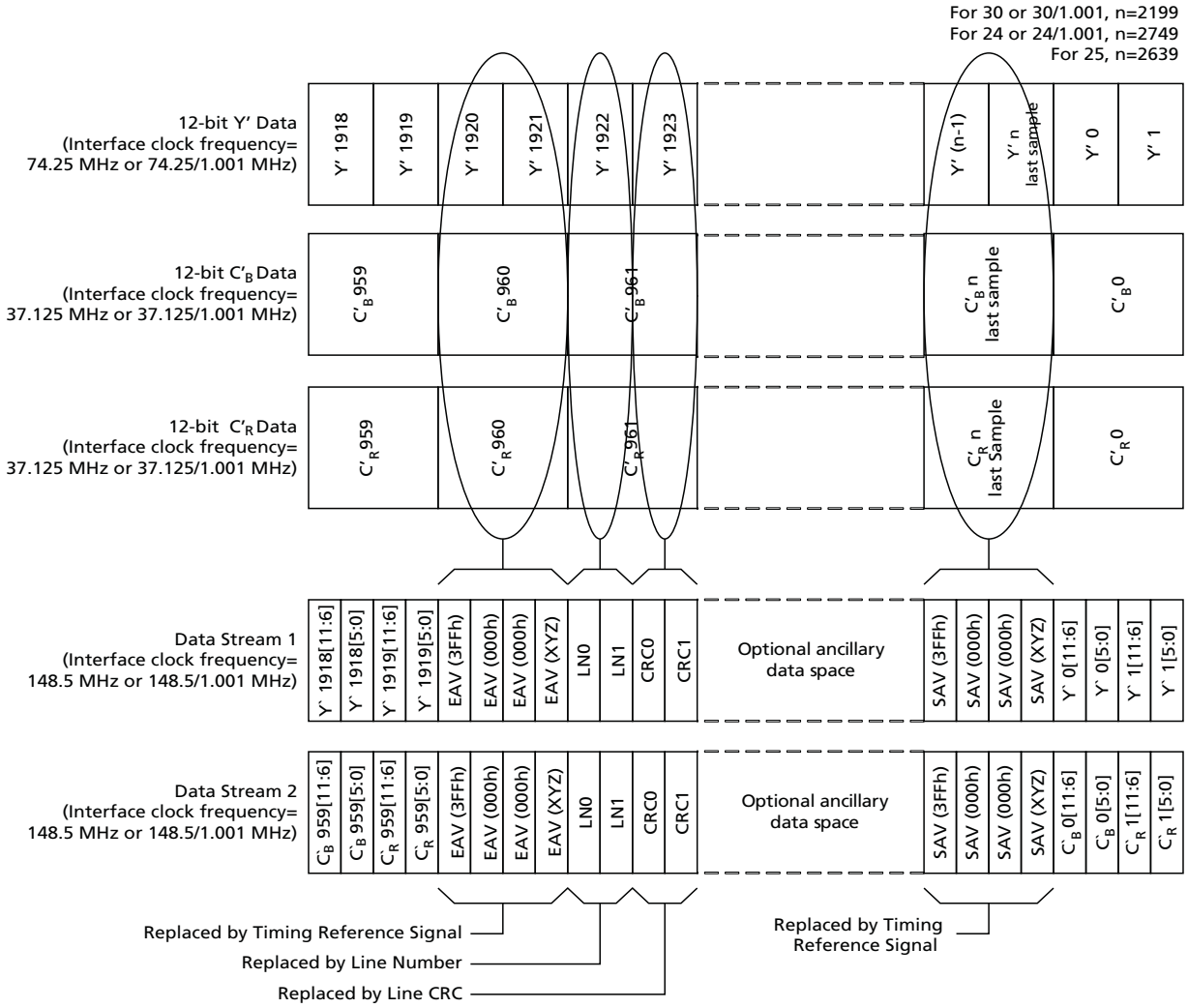


Figure 4-18: Aviia 20-bit Mapping Structure for 1920 x 1080 24/25/30Hz Progressive 4:2:2 (Y'C'$_B$C'$_R$) 12-bit Signals

Table 4-12: 1080p Y'C'$_B$C'$_R$ 4:2:2 12-bit Bit Structure Mapping

Bit Number										
Data Stream	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DS1 First Word	1	0	0	0	Y'[11:6]					
DS1 Second Word	1	0	0	0	Y'[5:0]					
DS2 First Word	1	0	0	0	C'$_B$[11:6]					
DS2 Second Word	1	0	0	0	C'$_B$[5:0]					
DS2 Third Word	1	0	0	0	C'$_R$[11:6]					
DS2 Fourth Word	1	0	0	0	C'$_R$[5:0]					

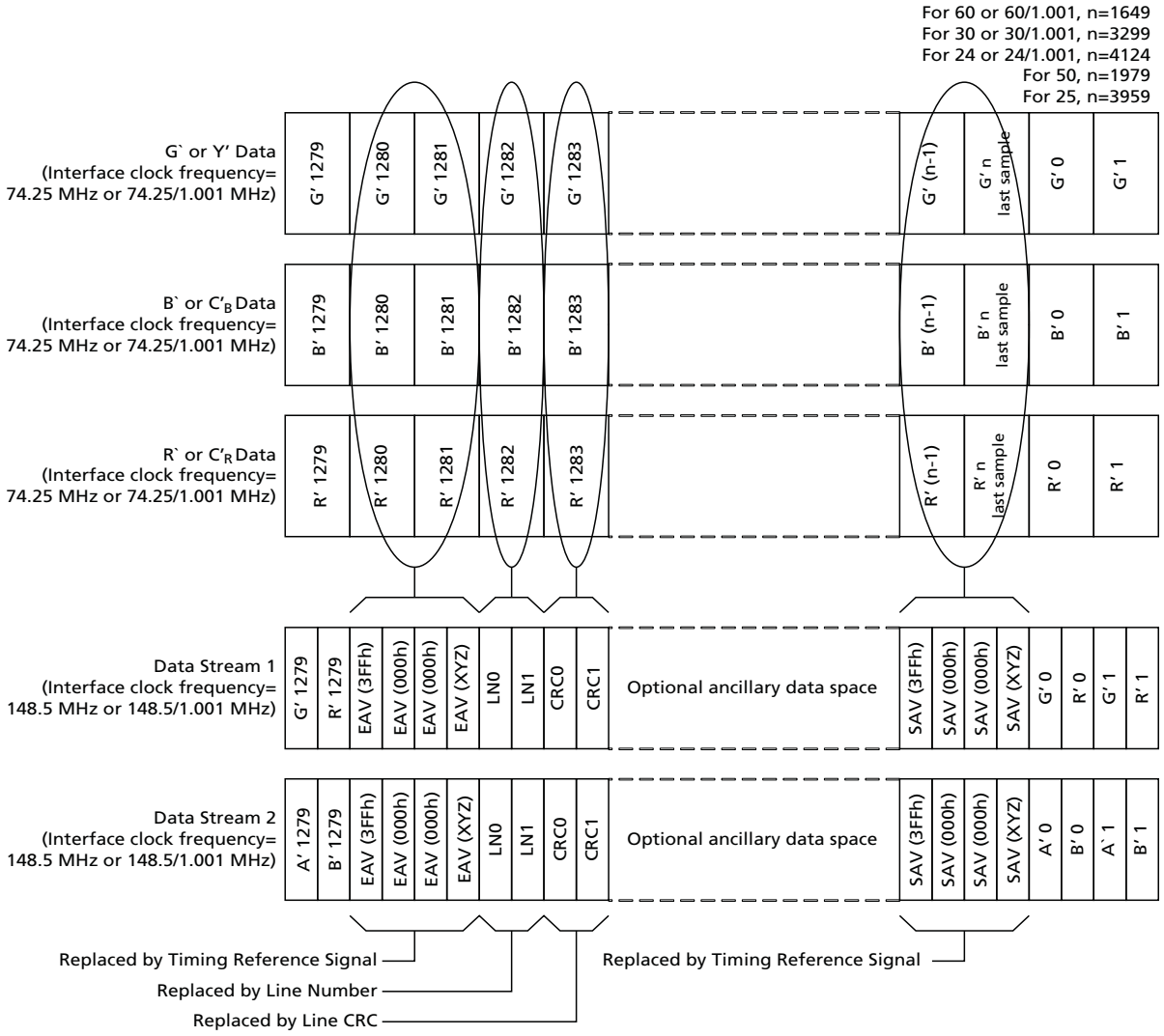


Figure 4-19: Aviia 20-bit Mapping Structure for 1280 x 720 24/25/30/25/60Hz Progressive 4:4:4 (R'G'B' or Y'C'$_B$C'$_R$) 8/10-bit Signals

Table 4-13: 720p R'G'B' or Y'C'$_B$C'$_R$ 4:4:4 10-bit Bit Structure Mapping

	Bit Number									
Data Stream	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DS1 First Word	G'[9:0] or Y'[9:0]									
DS1 Second Word	R'[9:0] or C'$_R$[9:0]									
DS2 First Word	A'[9:0]									
DS2 Second Word	B'[9:0] or C'$_B$[9:0]									

Note 1: The 10-bit 'A' data in Figure 4-19 is used to pad DS2 and should be set to 040h.

Note 2: For 8-bit systems, the data should be justified to the most significant bit (R'/C'$_R$9, G'/Y'9 and B'/C'$_B$9), with the two least significant bits (R'/C'$_R$[1:0], G'/Y'[1:0] and B'/C'$_B$[1:0]) set to zero.

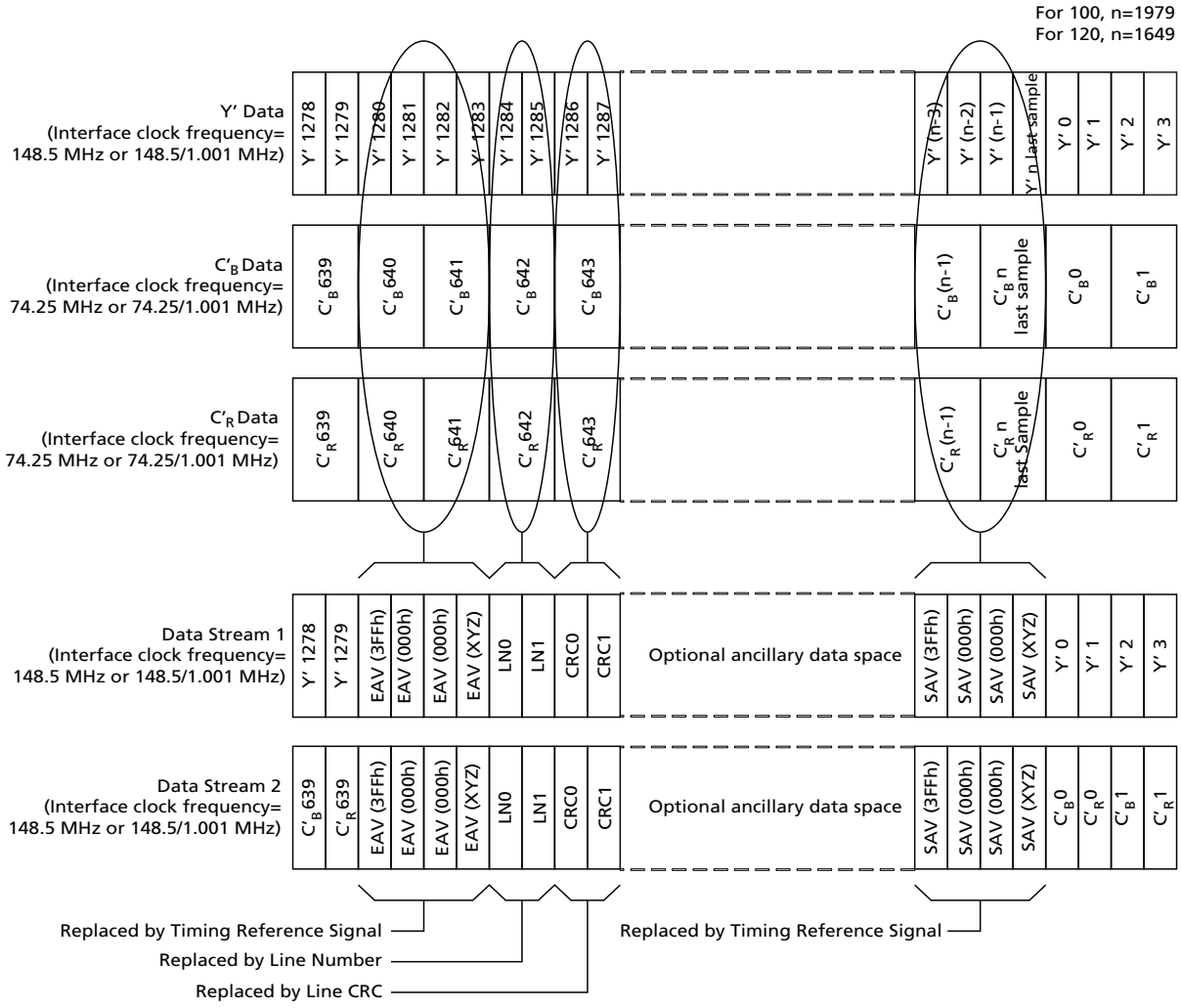


Figure 4-20: Aviia 20-bit Mapping Structure for 1280 x 720 100/120Hz Progressive 4:2:2 (Y'C'$_B$C'$_R$) 8/10-bit Signals

Table 4-14: 720p 100/120 Y'C'$_B$C'$_R$ 4:2:0 & 4:2:2 10-bit Bit Structure Mapping

	Bit Number									
Data Stream	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DS1	Y'[9:0]									
DS2	C'$_B$C'$_R$[9:0]									

Note: For 8-bit systems, the data should be justified to the most significant bit (Y'9 and C'$_B$C'$_R$9), with the two least significant bits (Y'[1:0] and C'$_B$C'$_R$[1:0]) set to zero.

4.2.1.6 Video Format & Bandwidth Requirements

Video data must be clocked into the GV7600 video data input bus at fixed pixel/data rates, which are directly related to the Aviia serial digital output rate. To support HD formats, the Aviia serial data rate is fixed at 1.485 Gb/s or 2.97 Gb/s. The device also supports these rates divided by 1.001. In order for a video format, which when serialized, to result in these fixed data rates, the following rule must be met:

Equation 4-1

$$\text{Total Pixels} \times \text{Total Lines} \times \text{Field/Frame Rate} \times \text{Number of Components*} \times 10 = \text{Aviia Serial Data Rate}$$

* For 4:2:2 sampled formats, the number of components is 2, one for Luma (Y') data and one for Chroma (C'$_B$C'$_R$) data. For 4:4:4 sampled formats, the number of components depends on bit-depth and the packing into Data Stream 1 and 2. See Section 4.2.1.5.

As an example, for a 1920 x 1080 30Hz progressive R'G'B' video format, the total raster must be 2200 x 1125 to meet the Aviia serial data rate, as follows:

$$2200 \times 1125 \times 30 \times 4 \times 10 = 2.97 \text{ Gb/s}$$

For non-HD image formats, such as VESA graphics formats, the total pixels and lines can be structured around the active image such that the pixel rate meets the above bandwidth requirements of the GV7600. Where the active image format fits inside the total HD raster, the horizontal and vertical timing can be adjusted such that the bandwidth requirements are met. This is illustrated in the following examples.

Example 4-1: Video Format for 2048x1536 at 15 frames per second

An R'G'B' sampled active image format of 2048 x 1536 at 15 frames per second requires the following serial data rate:

$$2048 \times 1536 \times 15 \times 4 \times 10 \; = \; 1.8874 \text{ Gb/s}$$

Both horizontal and vertical blanking can be added to "pad" the data rate up to the required 2.97 Gb/s serial data rate. The horizontal and vertical timing is shown in Figure 4-21.

$$3125 \times 1584 \times 15 \times 4 \times 10 \; = \; 2.97 \text{ Gb/s}$$

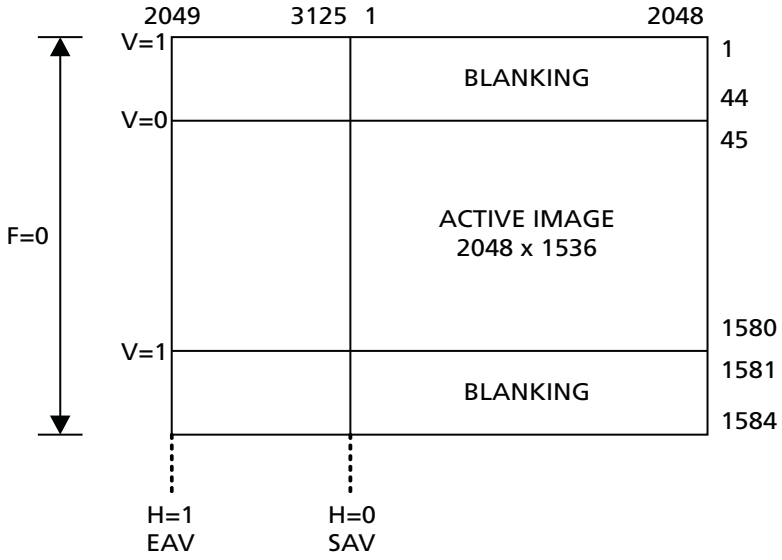


Figure 4-21: Timing for 2048 x 1536 15Hz Progressive

Example 4-2: Video Format for 1864 x 1050 at 30Hz

An active image format of 1864 x 1050 at 30Hz R'G'B' requires the following serial data rate:

$$1864 \times 1050 \times 30 \times 4 \times 10 \; = \; 2.34864 \text{ Gb/s}$$

Both horizontal and vertical blanking can be added to "pad" the data rate up to the total raster of a standard HD format, which results in a serial data rate of 2.97 Gb/s. The horizontal and vertical timing is shown in Figure 4-22.

$$2200 \times 1125 \times 30 \times 4 \times 10 \; = \; 2.97 \text{ Gb/s}$$

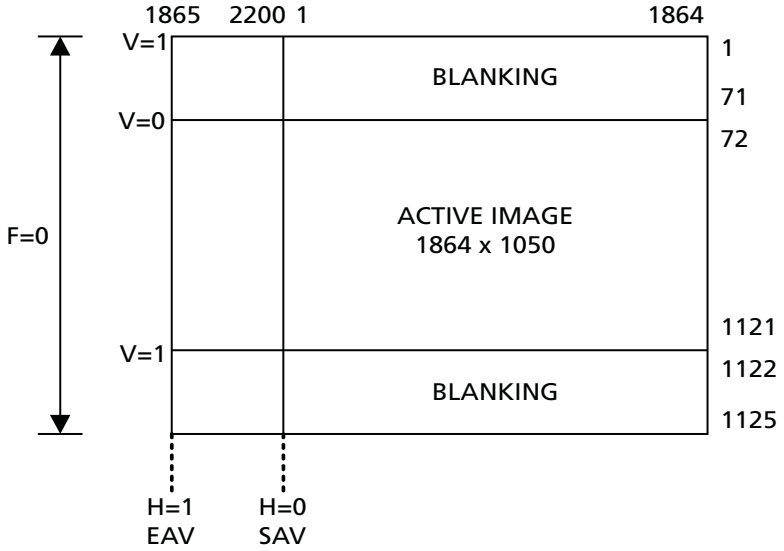


Figure 4-22: Timing for 1864 x 1050 30Hz Progressive

4.2.2 Parallel Input in ASI Mode

The GV7600 is in ASI mode with the $\overline{656\_BYPASS}$ pin is set LOW, the ASI pin is set HIGH, and the RATE_SEL0 pin is set HIGH. In this mode, all video processing features are disabled.

When operating in ASI mode, the device must be set to 10-bit mode by setting the 20BIT/$\overline{10BIT}$ pin LOW. The device accepts 8-bit transport stream data words on DIN[17:10], where DIN17 = HIN is the most significant bit of the transport stream data and DIN10 = AIN is the least significant bit. In addition, DIN19 and DIN18 are configured as the ASI control signals INSSYNCIN and KIN respectively.

DIN19 = INSSYNCIN
DIN18 = KIN
DIN17~10 = HIN ~ AIN where AIN is the least significant bit of the transport stream data.

4.2.3 Parallel Input in Data-Through Mode

Data-Through mode is enabled when the $\overline{656\_BYPASS}$ pin and the ASI pin are LOW.

In this mode, data at the input bus is serialized without any encoding, scrambling or word alignment taking place.

The input data width is controlled by the setting of the 20BIT/$\overline{10BIT}$ pin as shown in Table 4-2 above.

Note: When in HD 10-bit mode, asserting the $\overline{656\_BYPASS}$ pin LOW to put the device in data through mode creates video errors. If the user desires to use the device as a simple serializer in HD 10-bit mode, all video processing features must be disabled by setting the PROC_EN pin LOW.

4.2.4 Parallel Input Clock (PCLK)

The frequency of the PCLK input signal of the GV7600 is determined by the input data format and operating mode selection.

Table 4-15 below lists the input PCLK rates and input signal formats according to the external selection pins for the GV7600.

Table 4-15: GV7600 PCLK Input Rates

Input Data Format	Pin Settings					PCLK Rate
	20BIT/$\overline{10BIT}$	RATE_SEL0	RATE_SEL1	$\overline{656\_BYPASS}$	ASI	
20-bit demultiplexed Full HD format	HIGH	LOW	HIGH	HIGH	X	148.5 or 148.5/1.001MHz
20-bit demultiplexed HD format	HIGH	LOW	LOW	HIGH	X	74.25 or 74.25/1.001MHz
20-bit data Input Full HD format	HIGH	LOW	HIGH	LOW	LOW	148.5 or 148.5/1.001MHz
20-bit data input HD format	HIGH	LOW	LOW	LOW	LOW	74.25 or 74.25/1.001MHz
20-bit demultiplexed SD format	HIGH	HIGH	X	HIGH	LOW	13.5MHz
20-bit data input SD format	HIGH	HIGH	X	LOW	LOW	13.5MHz
10-bit multiplexed Full HD DDR format	LOW	LOW	HIGH	HIGH	LOW	148.5 or 148.5/1.001MHz
10-bit multiplexed HD format	LOW	LOW	LOW	HIGH	LOW	148.5 or 148.5/1.001MHz
10-bit data input HD format	LOW	LOW	LOW	LOW	LOW	148.5 or 148.5/1.001MHz

Table 4-15: GV7600 PCLK Input Rates (Continued)

Input Data Format	Pin Settings					PCLK Rate
	20BIT/$\overline{10BIT}$	RATE_SEL0	RATE_SEL1	$\overline{656\_BYPASS}$	ASI	
10-bit multiplexed SD format	LOW	HIGH	X	HIGH	X	27MHz
10-bit data input SD format	LOW	HIGH	X	LOW	LOW	27MHz
10-bit ASI input	LOW	HIGH	X	LOW	HIGH	27MHz

4.3 Video Mode

The function of this block is to carry out data scrambling according to ITU-R BT.656 and BT.1120, and to carry out NRZ to NRZI encoding prior to presentation to the parallel to serial converter.

These functions are only enabled when the $\overline{656\_BYPASS}$ pin is HIGH.

In addition, the GV7600 requires the ASI pin to be set LOW to enable this feature.

4.3.1 H:V:F Timing

In video mode, the GV7600 can automatically detect the video standard and generate all internal timing signals. The total line length, active line length, total number of lines per field/frame and total active lines per field/frame are calculated for the received parallel video.

When DETECT_TRS is LOW, the video standard and timing signals are based on the externally supplied horizontal blanking, vertical blanking, and field identification signals. These signals go to the H/HSYNC, V/VSYNC and F/DE pins respectively. When DETECT_TRS is HIGH, the video standard timing signals are extracted from the embedded TRS ID words in the parallel input data. Both 8-bit and 10-bit TRS code words are identified by the device.

Note: Video processing must be enabled for the device to remap 8-bit TRS words to the corresponding 10-bit value for transmission.

The GV7600 determines the video standard by timing the horizontal and vertical reference information supplied at the H/HSYNC, V/VSYNC, and F/DE input pins, or contained in the TRS ID words of the received video data. Therefore, full synchronization to the received video standard requires at least one complete video frame.

Once synchronization has been achieved, the GV7600 continues to monitor the received TRS timing or the supplied H, V, and F timing information to maintain synchronization. The GV7600 loses all timing information immediately following loss of H, V and F.

The H signal timing should also be configured via the H_CONFIG bit of the internal PROC_DISABLE register as either active line based blanking or TRS based blanking.

Active line based blanking is enabled when the H_CONFIG bit is set LOW. In this mode, the H input should be HIGH for the entire horizontal blanking period, including the EAV and SAV TRS words. This is the default H timing used by the device.

The timing of these signals is shown in Figure 4-23 to Figure 4-27 below.

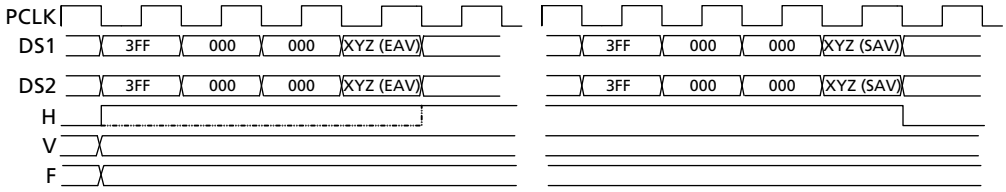


Figure 4-23: H:V:F Input Timing - Full HD 20-bit Input Mode

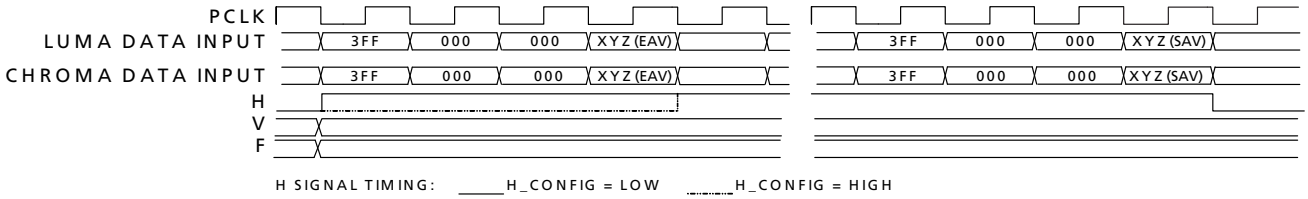


Figure 4-24: H:V:F Input Timing - HD 20-bit Input Mode

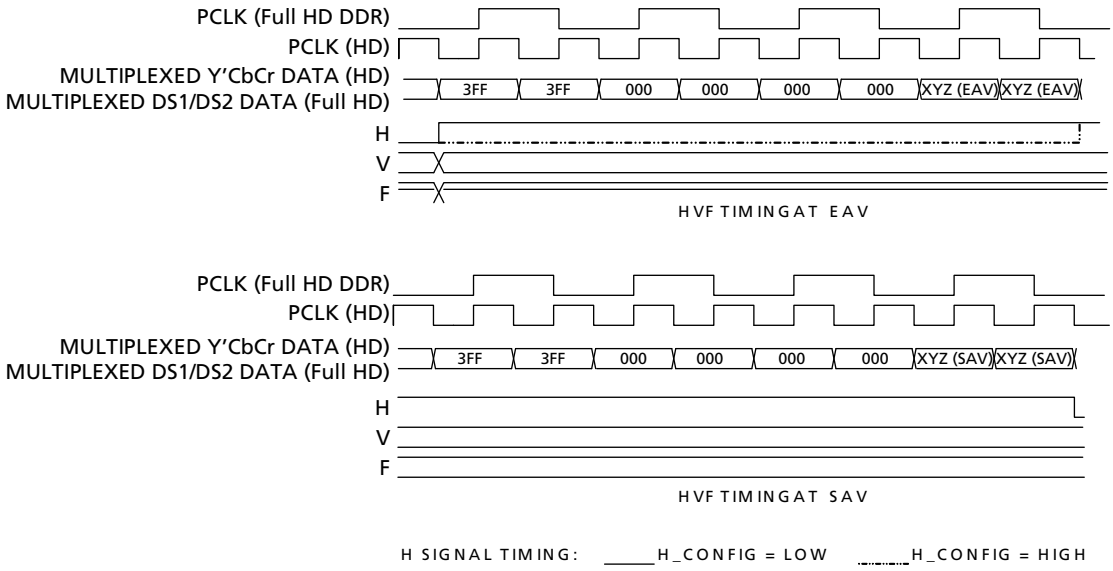


Figure 4-25: H:V:F Input Timing - HD & Full HD 10-bit Input Mode

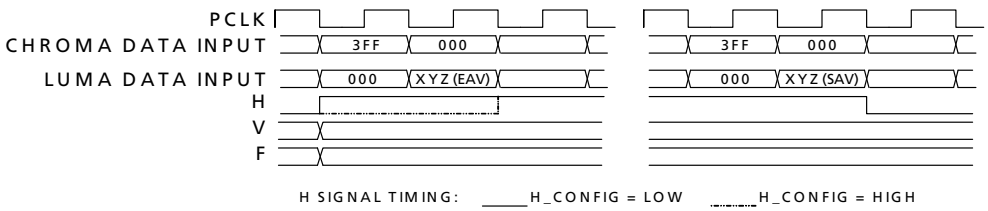


Figure 4-26: H:V:F Input Timing - SD 20-bit Mode

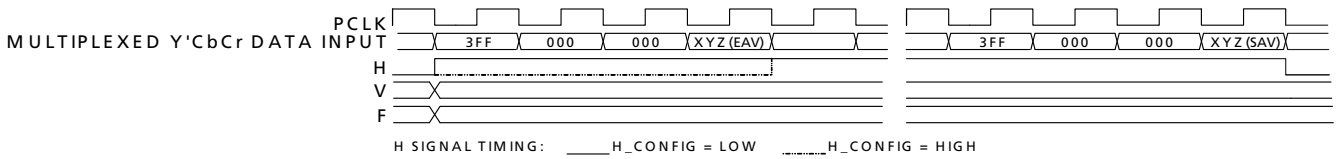


Figure 4-27: H:V:F Input Timing - SD 10-bit Mode

4.3.2 CEA-861 Timing

The GV7600 extracts timing information from externally provided HSYNC, VSYNC, and DE signals. When CEA-861 timing mode is selected by setting DETECT_TRS = LOW and 861_EN = HIGH, Horizontal Sync (H), Vertical Sync (V), and Data Enable (DE) timing must be provided via the H/HSYNC, V/VSYNC and F/DE input pins. The host interface register bit H_CONFIG is ignored in CEA-861 input timing mode.

The GV7600 determines the CEA-861 standard and embeds EAV and SAV TRS words in the output serial video stream.

Video standard detection is not dependent on the HSYNC pulse width or the VSYNC pulse width and therefore the GV7600 tolerates non-standard pulse widths. In addition, the device can compensate for up to ±1 PCLK cycle of jitter on VSYNC with respect to HSYNC and sample VSYNC correctly.

Note 1: The period between the leading edge of the HSYNC pulse and the leading edge of Data Enable (DE) must follow the timing requirements described in the CEA-861 specification. The GV7600 embeds TRS words according to this timing relationship to maintain compatibility with the corresponding ITU standard.

Note 2: When CEA-861 standards 6 & 7 [720(1440)x480i] are presented to the GV7600, the device embeds TRS words corresponding to the timing defined in ITU-R BT.656.

CEA-861 standards 6 & 7 [720(1440)x480i] define the active area on lines 22 to 261 and 285 to 524 inclusive (240 active lines per field). ITU-R BT.656 defines the active area on lines 20 to 263 and 283 to 525 inclusive (244 lines on field 1, 243 lines on field 2).

Therefore, in the first field, the GV7600 adds two active lines above and two active lines below the original active image. In the second field, it adds two lines above and one line below the original active image.

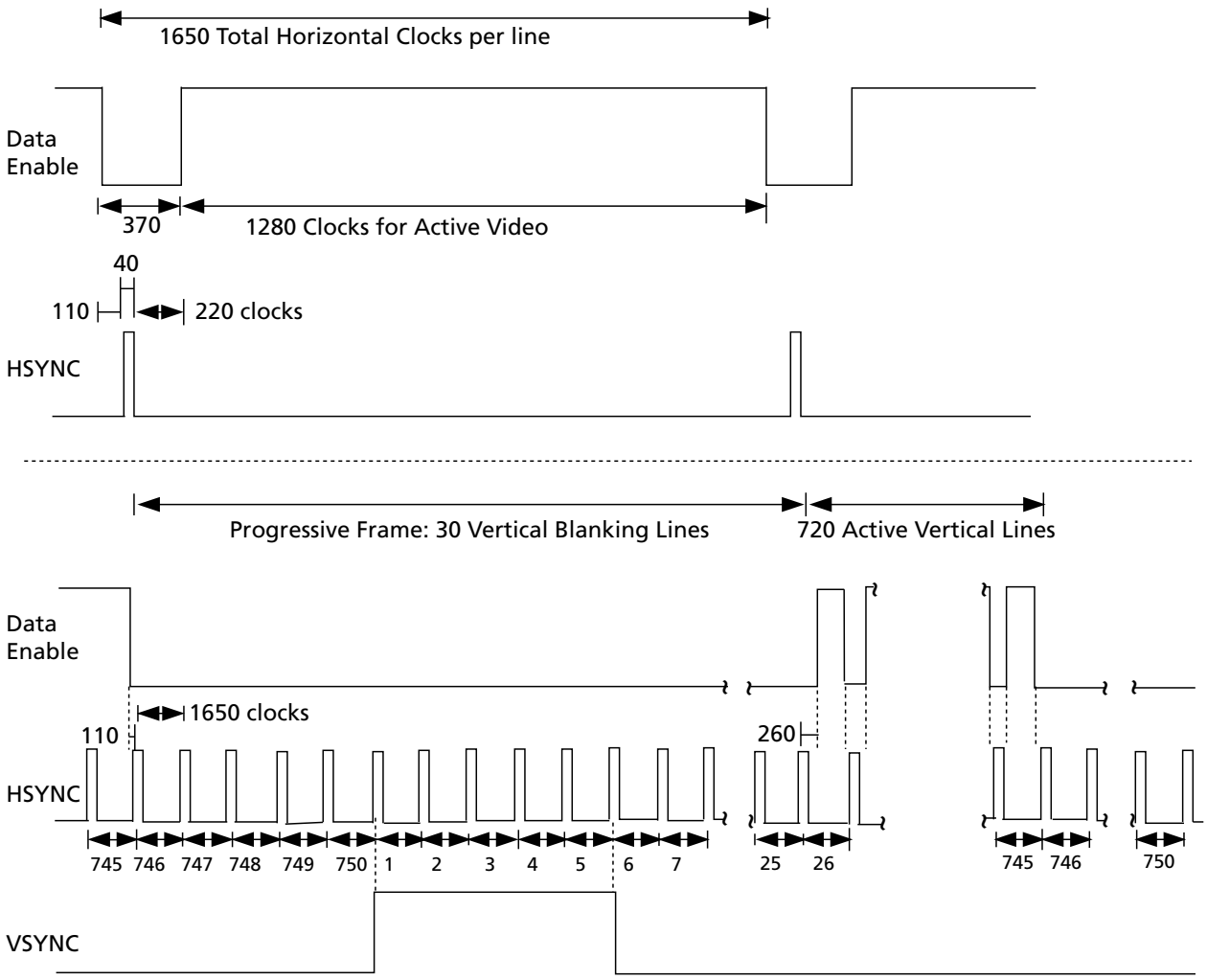


Figure 4-28: H:V:DE Input Timing 1280 x 720p @ 59.94/60 (Format 4)

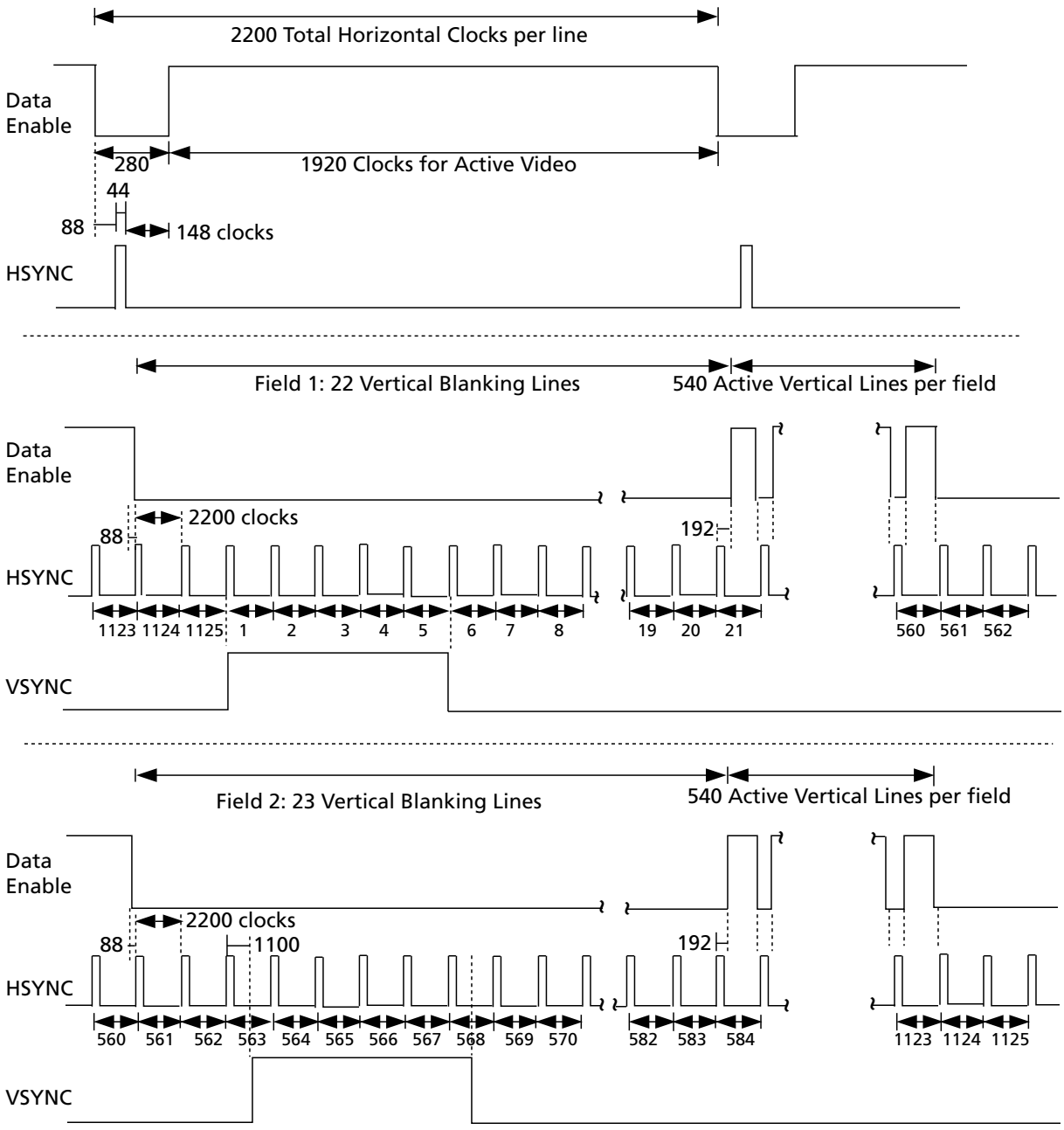


Figure 4-29: H:V:DE Input Timing 1920 x 1080i @ 59.94/60 (Format 5)

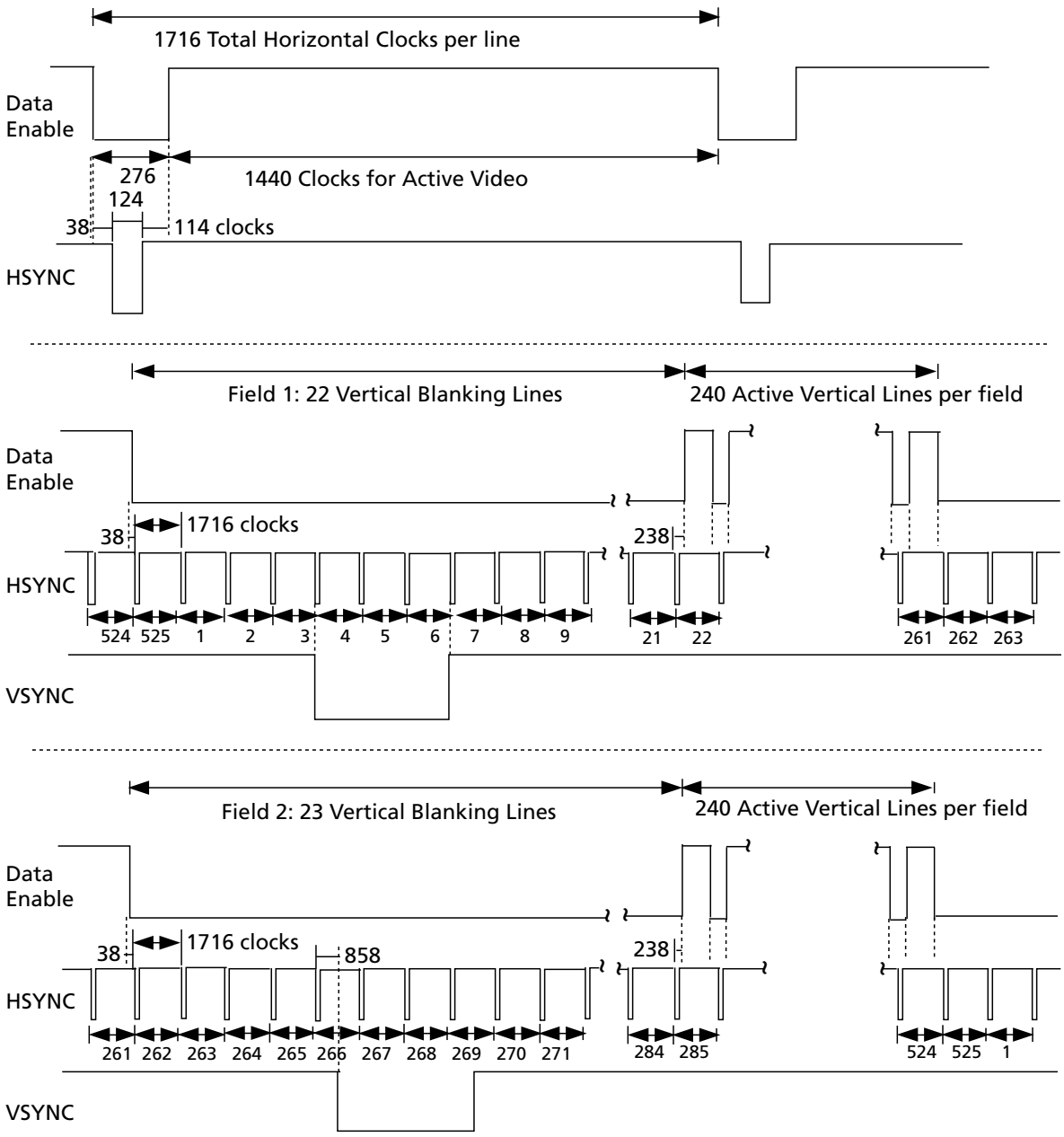


Figure 4-30: H:V:DE Input Timing 720 (1440) x 480i @ 59.94/60 (Format 6 & 7)

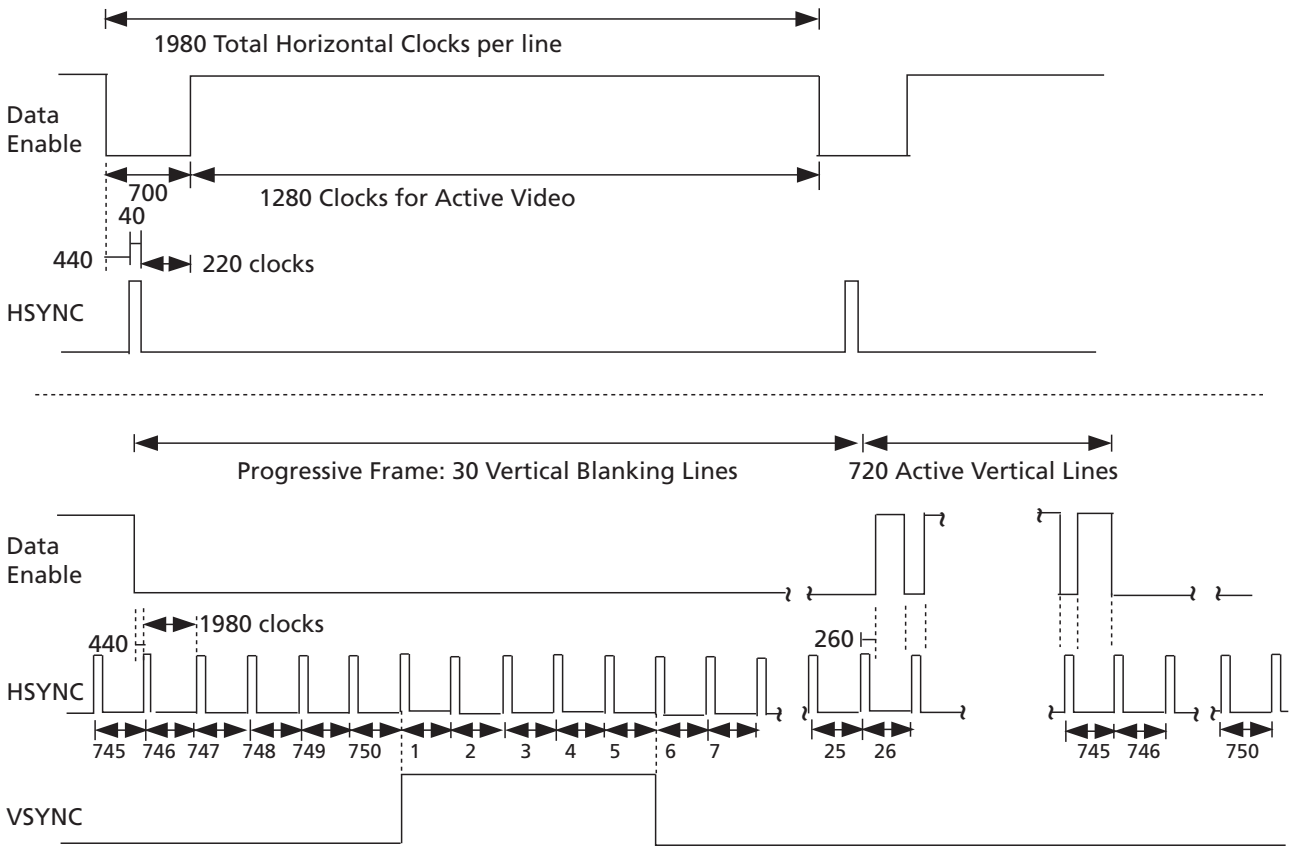


Figure 4-31: H:V:DE Input Timing 1280 x 720p @ 50 (Format 19)

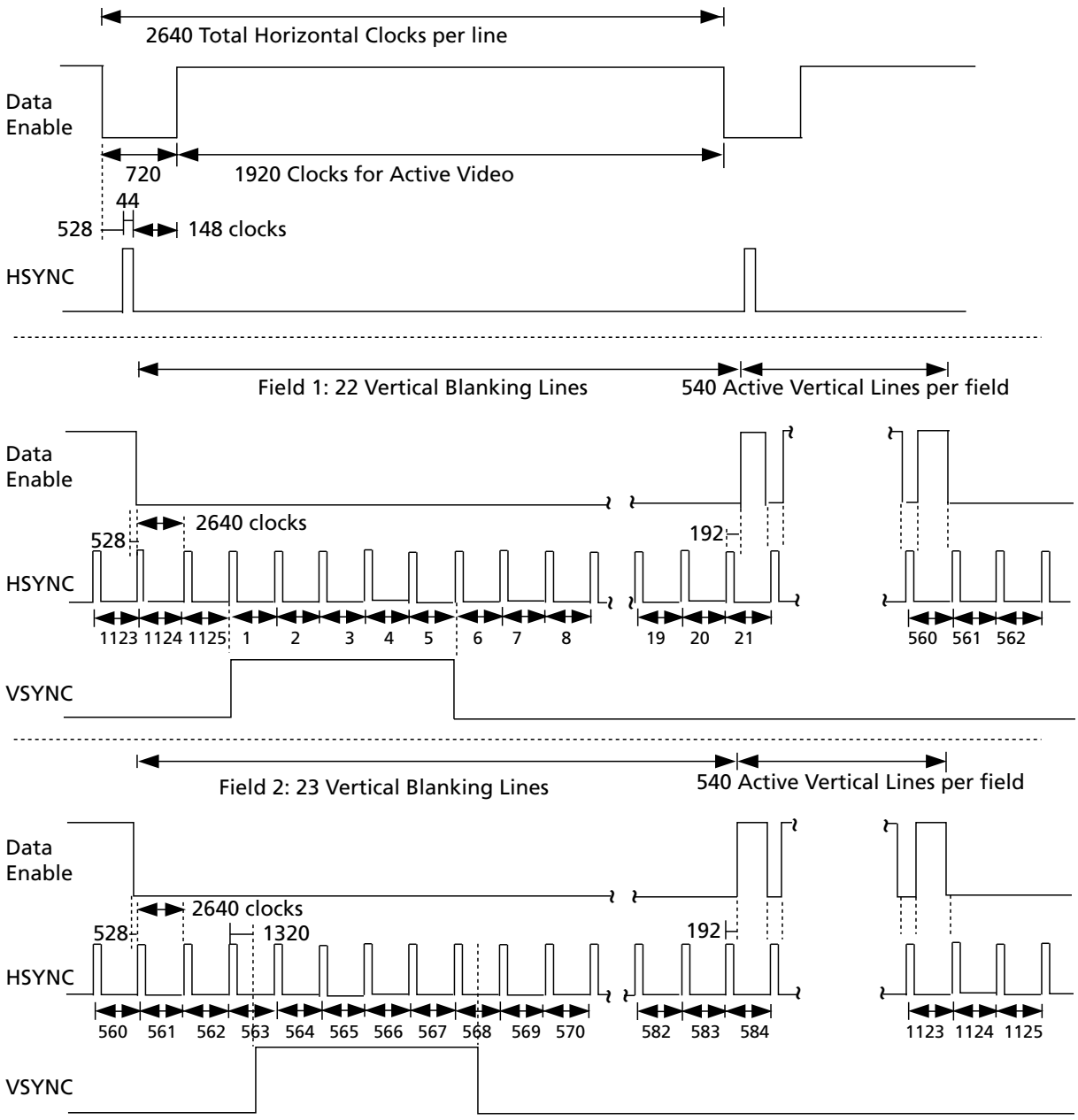


Figure 4-32: H:V:DE Input Timing 1920 x 1080i @ 50 (Format 20)

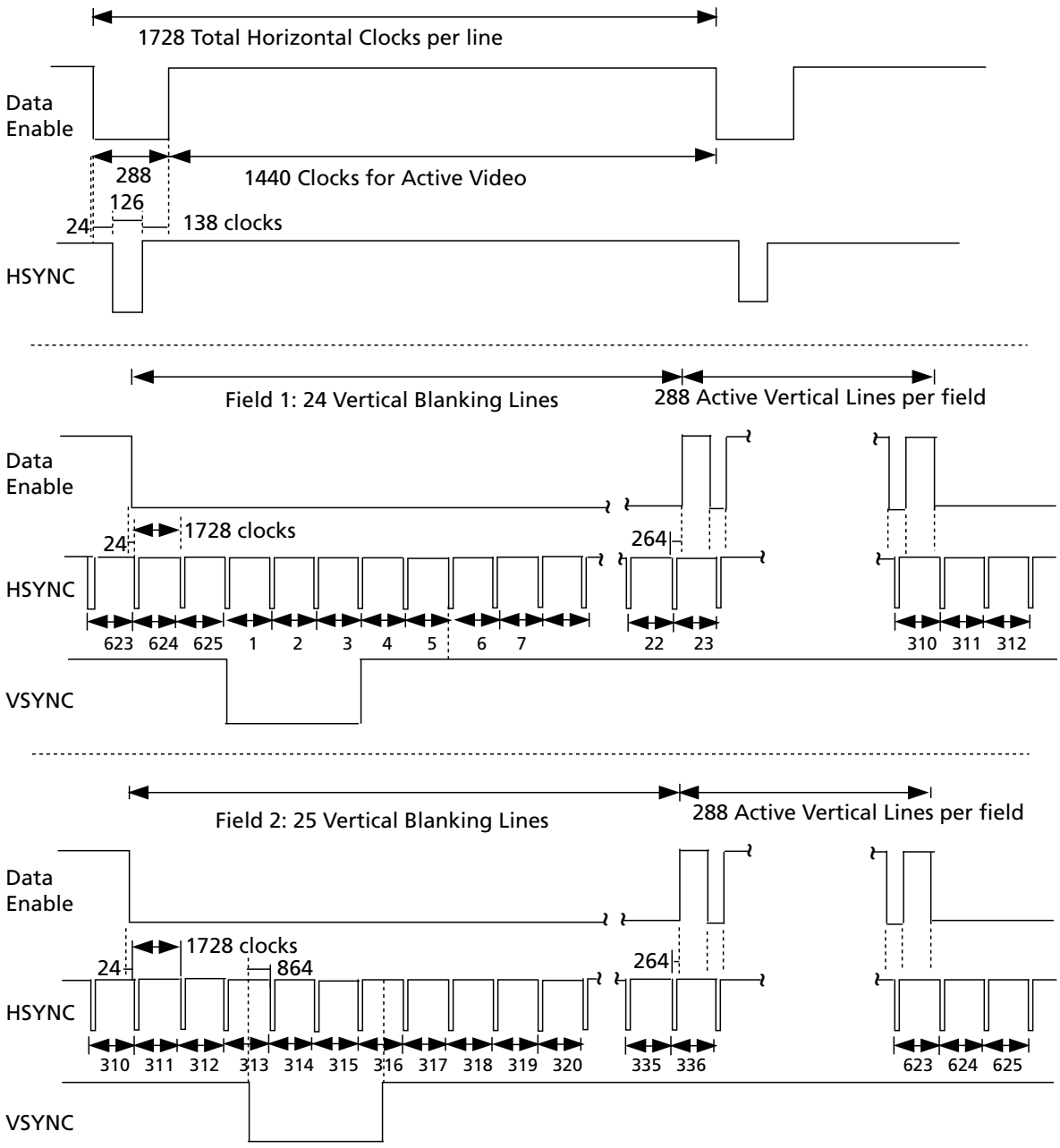


Figure 4-33: H:V:DE Input Timing 720 (1440) x 576 @ 50 (Format 21 & 22)

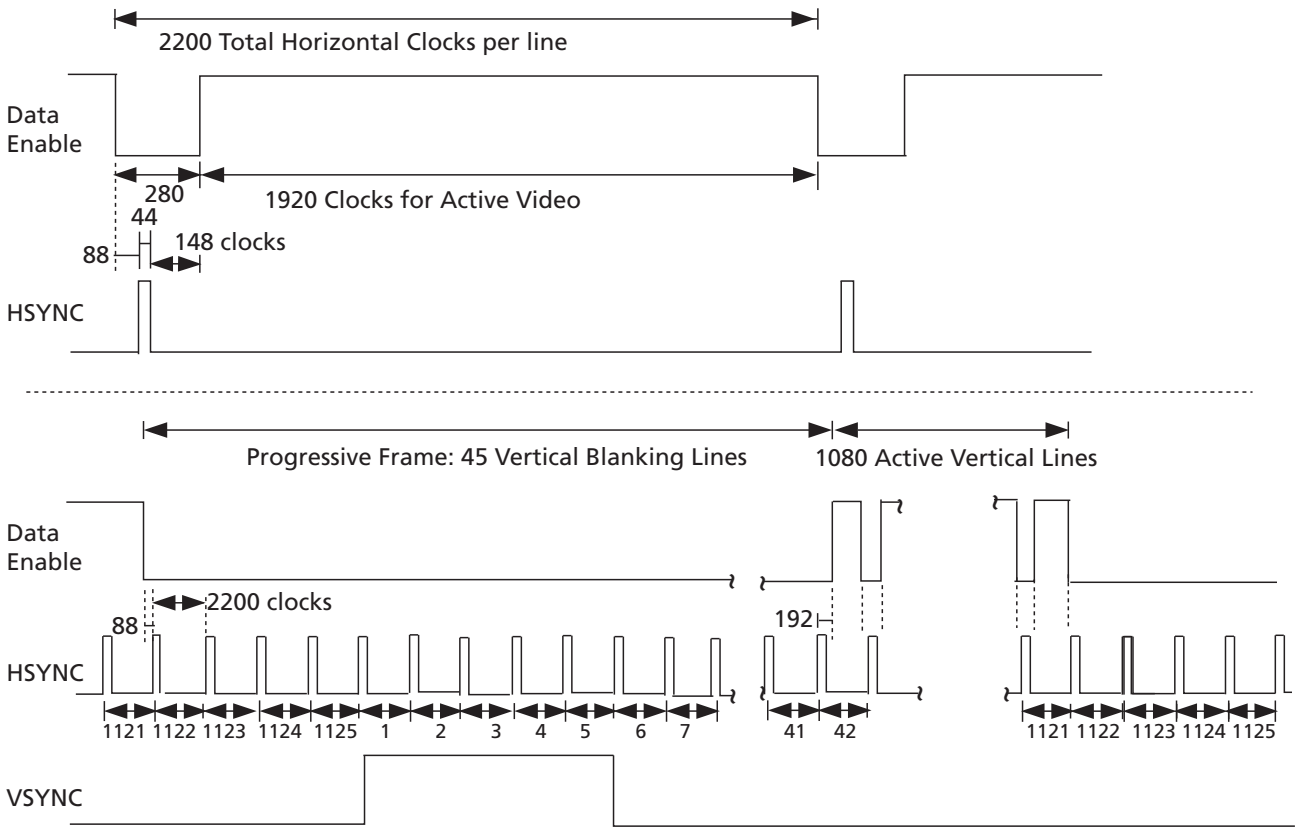


Figure 4-34: H:V:DE Timing 1920 x 1080p @ 59.94/60 (Format 16)

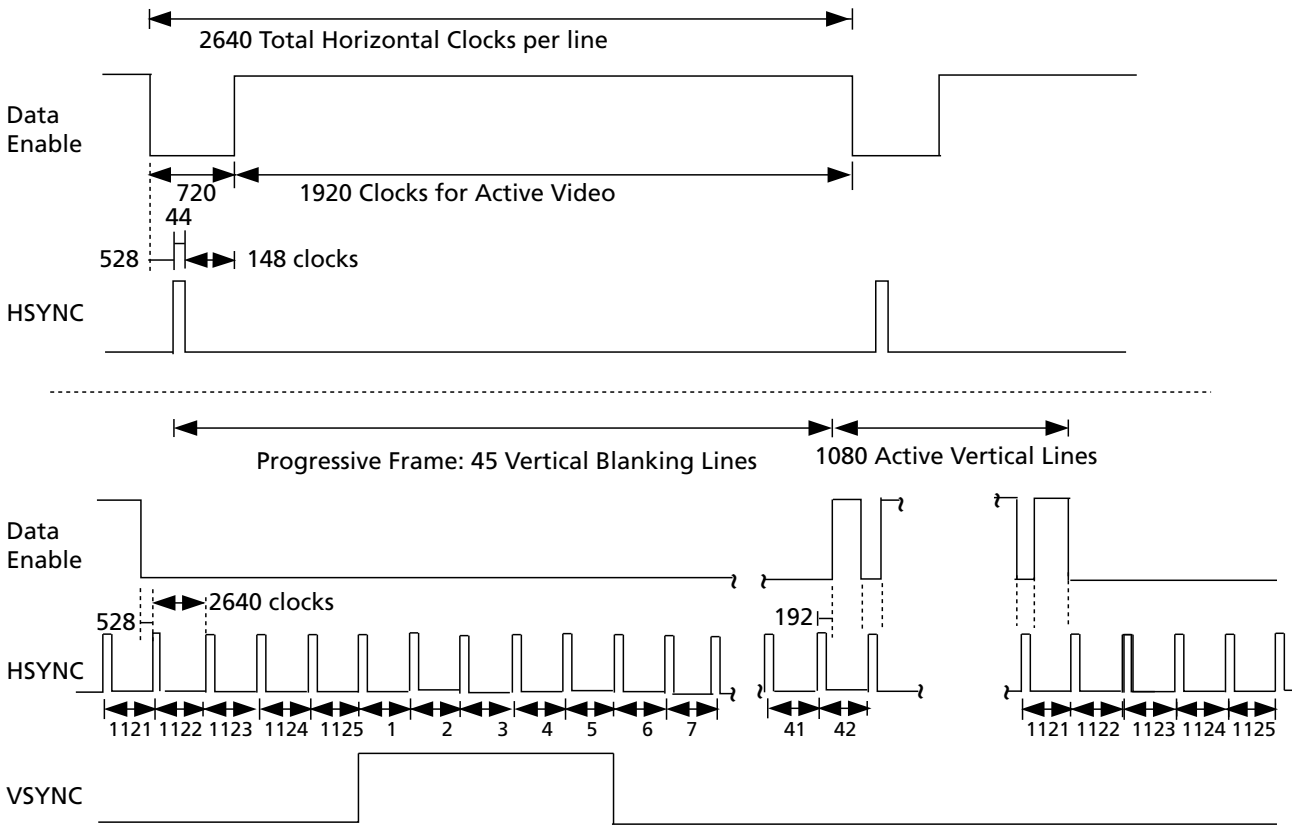


Figure 4-35: H:V:DE Timing 1920 x 1080p @ 50 (Format 31)

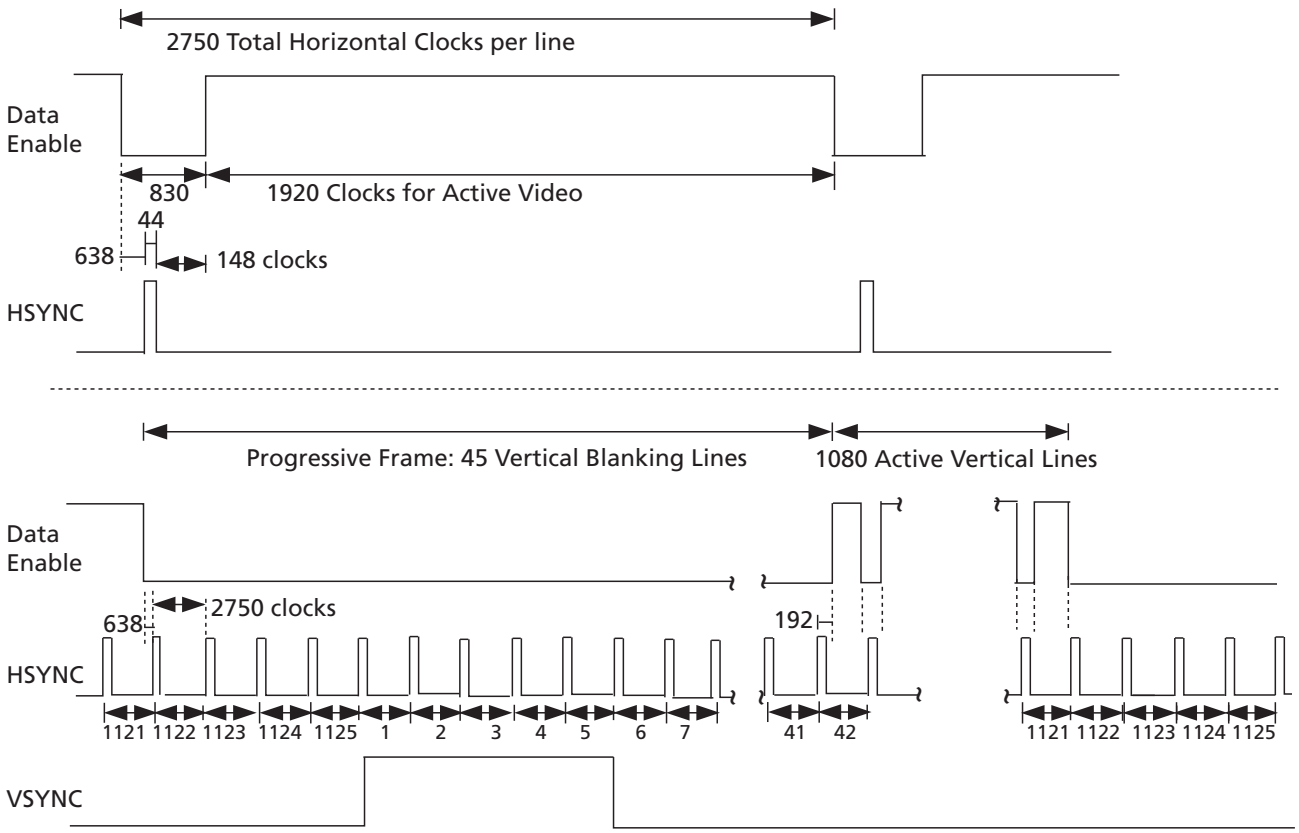


Figure 4-36: H:V:DE Timing 1920 x 1080p @ 23.94/24 (Format 32)

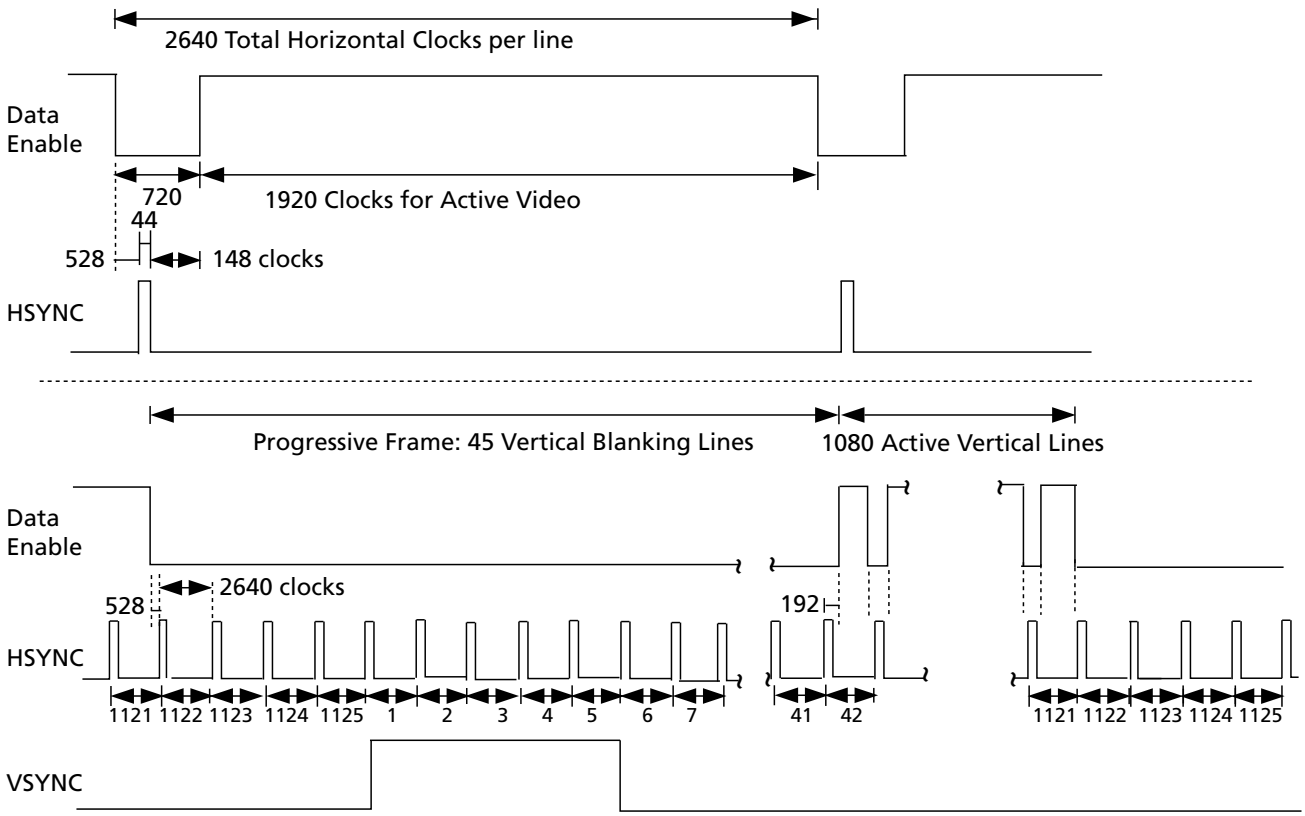


Figure 4-37: H:V:DE Timing 1920 x 1080p @ 25 (Format 33)

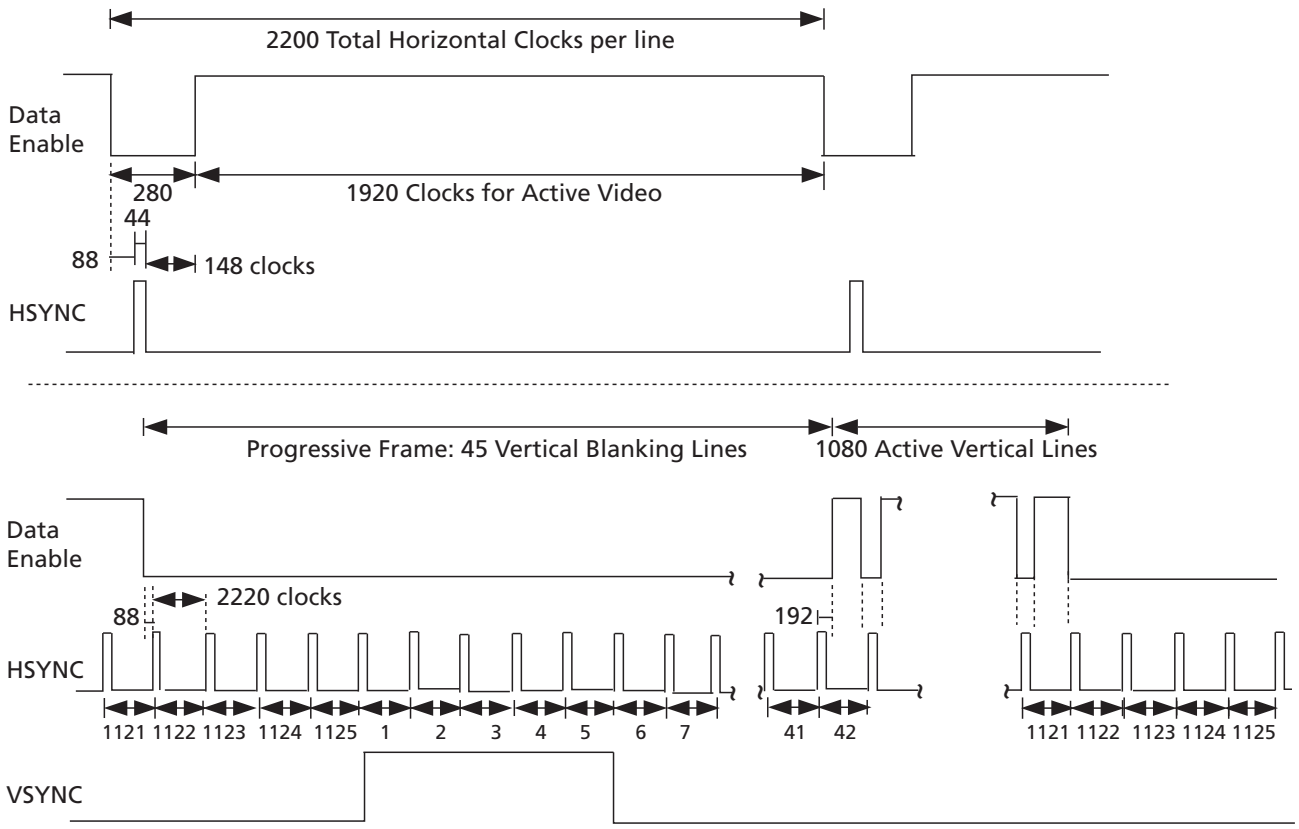


Figure 4-38: H:V:DE Timing 1920 x 1080p @ 29.97/30 (Format 34)

4.4 ASI Mode

When operating in ASI mode, all video processing features are disabled, and the device accepts 8-bit transport stream data and control signal inputs on the DIN[19:10] port.

This mode is only enabled when $\overline{656\_BYPASS}$ pin is LOW, ASI pin is HIGH and the RATE_SEL0 pin is HIGH.

The interface consists of eight data bits and two control signals, INSSYNCIN and KIN.

When INSSYNCIN is set HIGH, the GV7600 inserts K28.5 sync characters into the data stream. This function is used to assist system implementations where the GV7600 may be preceded by a data FIFO.

The FIFO can be fed data at a rate less than 27MHz. The 'FIFO empty' signal could be used to feed the INSSYNCIN pin, causing the GV7600 to pad the data up to the transmission rate of 27MHz.

When KIN is set HIGH the data input is interpreted as a special character (such as a K28.5 sync character), as defined by the EN 50083-9 standard. When KIN is set LOW, the input is interpreted as data.

After sync signal insertion, the GV7600 8b/10b encodes the data, generating a 10-bit data stream for the parallel to serial conversion and transmission process.

4.5 Data-Through Mode

The GV7600 may be configured to operate as a simple parallel-to-serial converter. In this mode, the device passes data to the serial output without performing any scrambling or encoding.

Data-Through mode is enabled when both the $\overline{656\_BYPASS}$ pin and the ASI pin are LOW.

4.6 Standby Mode

Setting the STANDBY pin HIGH reduces power to a minimum by disabling all circuits except for the register configuration. Upon setting the STANDBY pin back to LOW, the device returns to its previous operating condition within 1 second, without requiring input from the host interface.

Also in standby mode, the serial digital output signals becomes high-impedance.

4.7 Audio Embedding

The GV7600 includes an Audio Multiplexer, which by default is active when the device is configured for video mode. It can be disabled by setting the GRP1_EN and GRP2_EN pins LOW, or via the host interface. In non-video modes, the Audio Multiplexer is powered down to reduce device power.

Note: When audio is embedded by the GV7600, if either of the GRP1_EN or GRP2_EN pins are toggled, the output video stream is lost.

Toggling the audio disable pins on the fly must be avoided. The user has to set the pins before resetting the chip, and not change the setting during normal operation. The audio may be enabled or disabled during the operation of the chip by writing to the Host Interface registers. SD audio embedding may be enabled, or disabled, by writing to ACT1...ACT8 bits of register 40Fh. HD audio embedding may be enabled, or disabled, by writing to ACT1...ACT8 bits of register 80Eh.

4.7.1 Serial Audio Data Inputs

The GV7600 supports the insertion of up to 8 channels of embedded audio, in two groups of 4 channels.

Each audio group has a dedicated audio group enable input pin; a Word Clock (WCLK) input pin operating at 48kHz; an Audio Clock input pin (ACLK) operating at 3.072MHz (64 x WCLK); and two serial digital audio input pins (AIN1/2, etc.), supporting two channels of audio per pin.

The Serial Audio Data Inputs for each audio group are listed in Table 4-16.

Table 4-16: Serial Audio Input Pin Description

Pin Name	Description
Audio Group 1	
GRP1_EN	Enable Input for Channels 1-4
AIN1/2	Serial Audio Input; Channels 1 and 2
AIN3/4	Serial Audio Input; Channels 3 and 4
ACLK1	64 x clock for Channels 1-4
WCLK1	Word clock for Channels 1-4
Audio Group 2	
GRP2_EN	Enable Input for Channels 5-8
AIN5/6	Serial Audio Input; Channels 5 and 6
AIN7/8	Serial Audio Input; Channels 7 and 8
ACLK2	64 x clock for Channels 5-8
WCLK2	Word clock for Channels 5-8

The serial audio input signals and WCLK input signals enter the device on the rising edge of ACLK as shown in Figure 4-39.

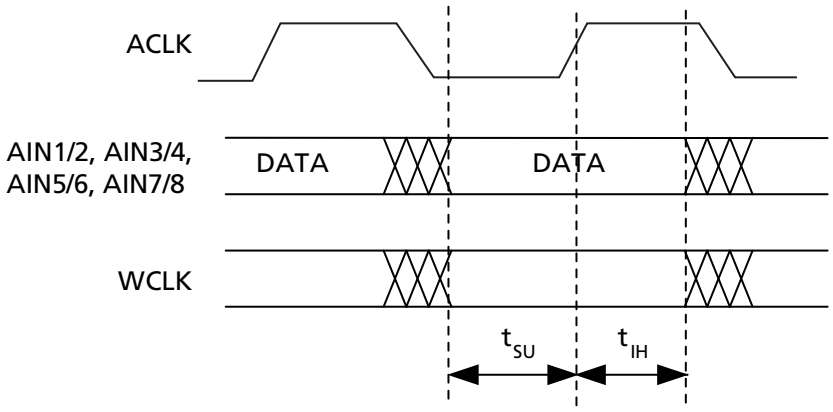


Figure 4-39: ACLK to Data and Control Signal Input Timing

Table 4-17: GV7600 Serial Audio Data Inputs - AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input data set-up time	t_{SU}	50% levels; 3.3v or 1.8v operation	1.3	–	–	ns
Input data hold time	t_{IH}		0.8	–	–	ns

When GRP1_ENand GRP2_EN are set HIGH, the respective audio group is enabled, and the audio input signals associated with that group are processed and embedded into the video data stream.

When GRP1_EN and GRP2_EN are set LOW, the respective audio group is disabled and the audio input signals associated with that group are ignored.

In addition, all functional logic associated with audio insertion for the disabled audio group is placed in a static operating mode, such that device power is reduced while the device configuration is retained.

4.7.2 Serial Audio Data Format Support

The GV7600 supports the following serial audio data formats:

- I^2S Audio (default)
- AES/EBU or S/PDIF
- Serial Audio, Left Justified, MSB First
- Serial Audio, Left Justified, LSB First
- Serial Audio, Right Justified, MSB First
- Serial Audio, Right Justified, LSB First

By default (at power up or after system reset), the I^2S data format is enabled. The other data formats are selectable via the host interface using the AMA/AMB/AMC/AMD[1:0] bits.

Table 4-18: Audio Input Formats

AMA/AMB/AMC/AMD[1:0]	Audio Output Formats
00	AES/EBU or S/PDIF audio output
01	Serial audio output: Left Justified; MSB first
10	Serial audio output: Right Justified; MSB first
11	I^2S (default)

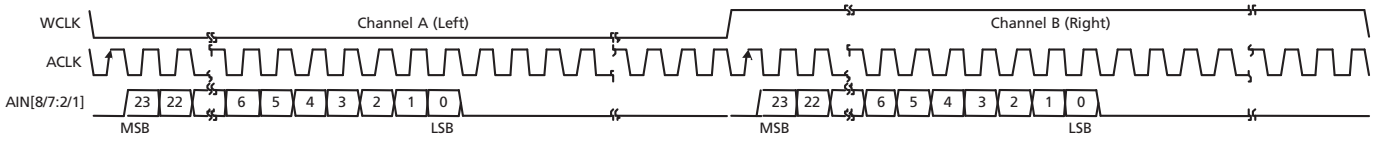


Figure 4-40: I^2S Audio Input Format

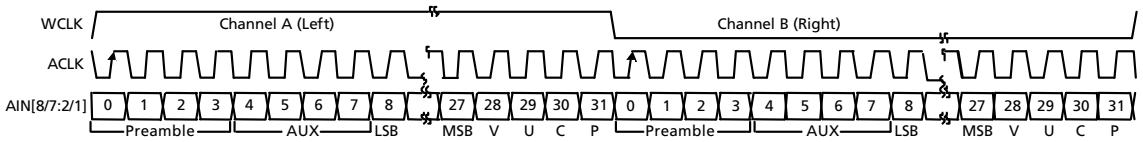


Figure 4-41: AES/EBU or S/PDIF Audio Input Format

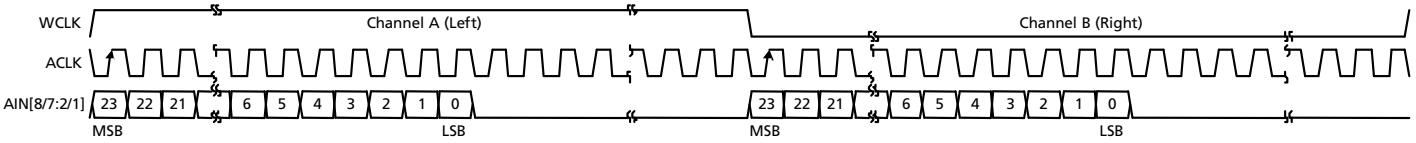


Figure 4-42: Serial Audio, Left Justified, MSB First

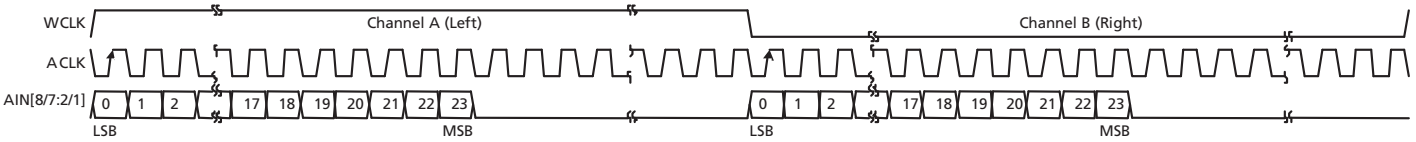


Figure 4-43: Serial Audio, Left Justified, LSB First

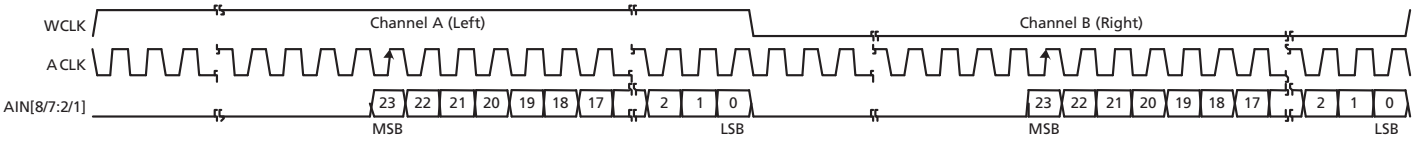


Figure 4-44: Serial Audio, Right Justified, MSB First

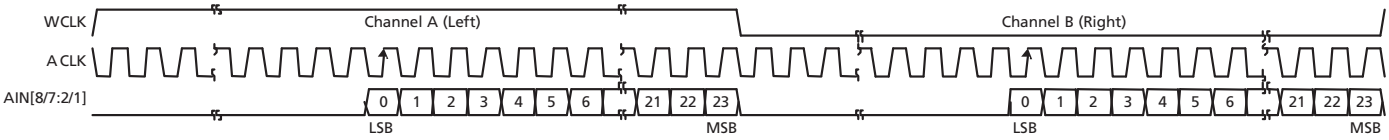


Figure 4-45: Serial Audio, Right Justified, LSB First

4.7.3 Audio Embedding Operating Modes

Audio Embedding operates in one of three distinct modes:

1. Normal Mode (Default)

All previously embedded audio packets are deleted from the video stream.
Up to two audio groups can be added to the video output.

2. Cascade Mode

No previously embedded packets are deleted from the video stream.
Up to two audio groups can be added to the video output.
The added audio groups will not replace existing embedded audio groups.
The added audio packets are appended to the last packet in the video input.

3. Group Replacement Mode

No previously embedded packets are deleted from the video stream.
Up to two audio groups can be added to the video output.
The added audio groups replace any embedded audio groups with the same group number.
The embedded audio groups are sorted in ascending order by audio group number.

The operating mode is selected using a combination of the EN_CASCADE and the AGR bits in the host interface, as stated in Table 4-19 below.

Table 4-19: GV7600 Audio Operating Mode Selection

Control Signals	Operating Mode
EN_CASCADE=0, AGR=0	Normal Mode
EN_CASCADE=1, AGR=0	Cascade Mode
EN_CASCADE=0, AGR=1	Group Replacement Mode
EN_CASCADE=1, AGR=1	Group Replacement Mode

4.7.4 Audio Packet Detection

The input video stream to the GV7600 may already contain embedded audio packets. The GV7600 detects these embedded packets, and signals their presence to the host interface.

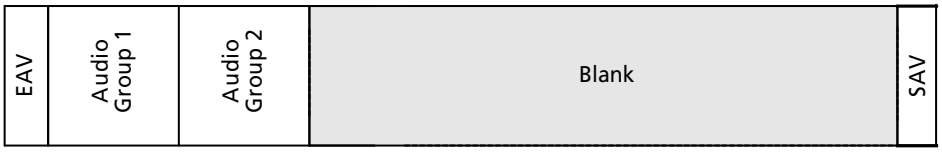
4.7.5 Audio Packet Detection and Deletion - SD Detail

In SD modes, the first Ancillary Data Flag (ADF) must always be contiguous after the EAV words. For HD mode, the first ADF must always be contiguous after the two line CRC words.

When CASCADE is set HIGH, all pre-existing audio data and control packets remain in the video stream.

When the AGR bit in the host interface is set HIGH, Audio Group Replacement mode is selected. In this mode, existing audio data and control packets are not deleted from the data stream. When Audio Group Replacement mode is selected, the CASCADE function is disabled.

In cases where the ADF is not placed immediately after the CRC or EAV words, or there are gaps between the packets, the device deletes all existing audio data and control packets, regardless of the CASCADE or AGR setting. Figure 4-46 shows an example of correct and incorrect placement of ancillary data packets in SD Mode.



Correct placement of Ancillary Data within HANC Space

HANC with space between EAV and Ancillary Data (Audio Packets will be deleted)

Figure 4-46: Ancillary Data Packet Placement Example

4.7.6 Audio Mute (Default Off)

The GV7600 mutes all of the input channels when the MUTE_ALL host interface bit is set HIGH.

The GV7600 mutes any individual audio inputs as commanded by the following host interface fields:

MUTE1 - Mute input channel 1

MUTE2 - Mute input channel 2

MUTE3 - Mute input channel 3

MUTE4 - Mute input channel 4

MUTE5 - Mute input channel 5

MUTE6 - Mute input channel 6

MUTE7 - Mute input channel 7

MUTE8 - Mute input channel 8

4.7.7 Audio Channel Status

The GV7600 adds audio channel status to those audio input channels that do not use the AES/EBU or S/PDIF format.

The Audio Channel Status block complies with the AES3-1992 (ANSI S4.40-1992) and IEC 60958 standards.

The GV7600 uses the ACSR[183:0] host interface field as the source of audio channel status for those input channels that do not use the AES/EBU or S/PDIF format.

The GV7600 replaces the Audio Channel Status block in all eight channels as commanded by the ACS_REGEN host interface bit. The status block information is supplied by the ACSR[183:0] host interface field.

The GV7600 does not use the ACSR[183:0] data until the ACS_APPLY host interface bit is set HIGH, and a new status boundary occurs.

The GV7600 asserts the APPLY_WAITA host interface bit between the time that ACS_APPLY is set and the time that the new status boundary occurs for the Primary audio group.

The GV7600 asserts the APPLY_WAITB host interface bit between the time that ACS_APPLY is set and the time that the new status boundary occurs for the Secondary audio group.

The GV7600 automatically calculates the CRC required for the Audio Channel Status block.

4.7.8 Audio Crosspoint

The GV7600 is capable of mapping any input channel to any Primary or Secondary group channel.

Each group channel specifies the audio source using a 3-bit selector defined below in Table 4-20:

Table 4-20: SD Audio Crosspoint Channel Selection

Audio Source	Selector
Input channel 1	000
Input channel 2	001
Input channel 3	010
Input channel 4	011
Input channel 5	100
Input channel 6	101
Input channel 7	110
Input channel 8	111

Each Primary and Secondary group channel specifies the audio source using the following host interface fields:

Table 4-21: Audio Source Host Interface Fields

Host Interface Field	Description	Default
GPA_CH1_SRC[2:0]	Primary Group Channel 1 Source Selector	000
GPA_CH2_SRC[2:0]	Primary Group Channel 2 Source Selector	001
GPA_CH3_SRC[2:0]	Primary Group Channel 3 Source Selector	010
GPA_CH4_SRC[2:0]	Primary Group Channel 4 Source Selector	011
GPB_CH1_SRC[2:0]	Secondary Group Channel 1 Source Selector	100
GPB_CH2_SRC[2:0]	Secondary Group Channel 2 Source Selector	101
GPB_CH3_SRC[2:0]	Secondary Group Channel 3 Source Selector	110
GPB_CH4_SRC[2:0]	Secondary Group Channel 4 Source Selector	111

Audio channels can be paired only when both channels are derived from the same Word Clock and are synchronous.

The same audio channel cannot be used in both Primary and Secondary groups at the same time.

The GV7600 asserts the XPOINT_ERROR host interface bit if any audio channel is programmed to be included in both the Primary and Secondary groups.

4.7.9 Audio Word Clock

When the GV7600 combines two stereo pair inputs into one audio group, the HD format allows for only one Word Clock, or sampling clock.

For the Primary group, the GV7600 uses the Word Clock associated with the source selected by the GPA_WCLK_SRC[2:0] host interface field.

For the Secondary group, the GV7600 uses the Word Clock associated with the source selected by the GPB_WCLK_SRC[2:0] host interface field.

For proper operation, the combined Stereo Pair inputs must have identical Word Clocks.

4.7.10 Channel & Group Activation

The GV7600 embeds Primary group packets when any of the following host interface bits are set and the associated audio group enable pin is HIGH:

ACT1 Embed Primary group audio channel 1
ACT2 Embed Primary group audio channel 2
ACT3 Embed Primary group audio channel 3
ACT4 Embed Primary group audio channel 4

If none of the bits are set, then no audio is embedded.

The GV7600 embeds Secondary group packets when any of the following host interface bits are set and the associated audio group enable pin is HIGH:

ACT5 Embed Secondary group audio channel 1
ACT6 Embed Secondary group audio channel 2
ACT7 Embed Secondary group audio channel 3
ACT8 Embed Secondary group audio channel 4

When an embedded packet contains one or more channels with the ACTx bit set to zero, the GV7600 replaces the data for those channels with null samples (all bits set to zero).

In the default state, the GV7600 embeds all audio channels in accordance with the setting of the respective audio group enable pins of the device.

4.7.11 ECC Error Detection and Correction

For audio embedding in HD video formats, the packetized audio sample data is protected for bit errors using error correction codes (ECC). The error correction codes are carried in the same packet as the audio sample data for error detection and correction in the Aviia receiver. The GV7600 uses BCH(31,25) code for ECC.

The GV7600 automatically generates the error detection and correction fields in the audio data packets.

4.7.12 Audio Control Packet Insertion - SD

The GV7600 embeds audio according to the Society of Motion Pictures and Television Engineers (SMPTE) 272M-2004 for standard definition video. SMPTE 272M defines an audio control packet, which is used to carry information about the audio sample data, such as audio sample rate, audio validity and audio-to-video timing relationship (delay).

The GV7600 automatically generates audio control packets. It is also possible to program audio control packet data via the host interface. For information on how the audio control data should be formatted, please consult the SMPTE 272M standard document.

The GV7600 embeds audio control packets associated with the Primary Group audio and the Secondary Group audio.

The Primary Group audio to be embedded is specified using the IDA[1:0] host interface field (Address 400h).

The Secondary Group audio to be embedded is specified using the IDB[1:0] host interface field.

The Primary Group audio control packets is embedded as commanded by the CTRA_ON host interface bit (default is ON).

The Secondary Group audio control packets is embedded as commanded by the CTRB_ON host interface bit (default is ON).

The Primary Group audio control packets is replaced as commanded by the CTR_AGR host interface bit (default is OFF).

The Secondary Group audio control packets is replaced as commanded by the CTR_AGR and ONE_AGR host interface bits (default is OFF).

The contents of the Primary Group audio control packet is specified using the following host interface fields:

AFNA_AUTO Primary Group audio frame number generation.
EBIT1A Primary Group delay valid flag for channel 1.
DEL1A[25:0] Primary Group delay for channel 1.
EBIT2A Primary Group delay valid flag for channel 2.
DEL2A[25:0] Primary Group delay for channel 2.
EBIT3A Primary Group delay valid flag for channel 3.
DEL3A[25:0] Primary Group delay for channel 3.
EBIT4A Primary Group delay valid flag for channel 4.
DEL4A[25:0] Primary Group delay for channel 4.

The contents of the Secondary Group audio control packet is specified using the following host interface fields:

AFNB_AUTO Secondary Group audio frame number generation.
EBIT1B Secondary Group delay valid flag for channel 1.
DEL1B[25:0] Secondary Group delay for channel 1.
EBIT2B Secondary Group delay valid flag for channel 2.
DEL2B[25:0] Secondary Group delay for channel 2.
EBIT3B Secondary Group delay valid flag for channel 3.
DEL3B[25:0] Secondary Group delay for channel 3.
EBIT4B Secondary Group delay valid flag for channel 4.
DEL4B[25:0] Secondary Group delay for channel 4.

4.7.13 Audio Control Packet Insertion - HD

For HD video formats, the GV7600 embeds audio according to the Society of Motion Pictures and Television Engineers (SMPTE) 299M-2004. The SMPTE 299M standard defines an audio control packet, which is used to carry information about the audio sample data, such as audio sample rate, audio validity, audio synchronization, and audio-to-video timing relationship (delay).

The GV7600 automatically generates and embeds audio control packets. It is also possible to program audio control packet data via the host interface. For information on how the audio control data should be formatted, please consult the SMPTE 299M standard document.

The GV7600 embeds audio control packets associated with the Primary Group audio and the Secondary Group audio.

The Primary Group audio to be embedded is specified using the IDA[1:0] host interface field (default is 00 in NORMAL mode).

The Secondary Group audio to be embedded is specified using the IDB[1:0] host interface field (default is 01 in NORMAL mode).

The Primary Group audio control packets are embedded as commanded by the CTRA_ON host interface bit (default is 1).

The Secondary Group audio control packets are embedded as commanded by the CTRB_ON host interface bit (default is 1).

The Primary Group audio control packets are replaced as commanded by the CTR_AGR host interface bit (default is 0).

The Secondary Group audio control packets are replaced as commanded by the CTR_AGR and ONE_AGR host interface bits (default is 0).

The Primary Group audio control packets are not embedded or replaced unless one or more of the ACT1, ACT2, ACT3 or ACT4 host interface bits are set.

The Secondary Group audio control packets are not embedded or replaced unless one or more of the ACT5, ACT6, ACT7 or ACT8 host interface bits are set.

The contents of the Primary Group audio control packet is specified using the following host interface fields:

AFNA_AUTO - Primary Group audio frame number auto-generation.
ASXA - Primary Group asynchronous mode.
DEL1_2A[25:0] - Primary Group audio delay for channels 1 and 2.
DEL3_4A[25:0] - Primary Group audio delay for channels 3 and 4.

The contents of the Secondary Group audio control packet is specified using the following host interface fields:

AFNB_AUTO - Secondary Group audio frame number auto-generation.
ASXB - Secondary Group asynchronous mode.
DEL1_2B[25:0] - Secondary Group audio delay for channels 1 and 2.
DEL3_4B[25:0] - Secondary Group audio delay for channels 3 and 4.

4.7.14 Audio Interrupt Control

The GV7600 asserts the interrupt signal when an internal interrupt condition becomes true and the type of interrupt is enabled.

The following host interface bits enable the various interrupt sources:

Table 4-22: Audio Interrupt Control – Host Interface Bit Description

Bit Name	Description
EN_NO_VIDEO	Asserts interrupt when video format is unknown
EN_ACPG1_DET	Asserts interrupt when ACPG1_DET flag is set
EN_ACPG2_DET	Asserts interrupt when ACPG2_DET flag is set
EN_ACPG3_DET	Asserts interrupt when ACPG3_DET flag is set
EN_ACPG4_DET	Asserts interrupt when ACPG4_DET flag is set
EN_ADPG1_DET	Asserts interrupt when ADPG1_DET flag is set
EN_ADPG2_DET	Asserts interrupt when ADPG2_DET flag is set
EN_ADPG3_DET	Asserts interrupt when ADPG3_DET flag is set
EN_ADPG4_DET	Asserts interrupt when ADPG4_DET flag is set
EN_AES_ERRA	Asserts interrupt when AES_ERRA flag is set
EN_AES_ERRB	Asserts interrupt when AES_ERRB flag is set
EN_AES_ERRC	Asserts interrupt when AES_ERRC flag is set
EN_AES_ERRD	Asserts interrupt when AES_ERRD flag is set

By default, the interrupts are all disabled.

4.8 Ancillary Data Insertion

The horizontal and vertical blanking regions of a digital video signal may be used to carry ancillary data packets. The payload of the ancillary data packet can be used to carry user-defined or proprietary data, which can be sent between an Aviia transmitter and receiver.

The ancillary data packet must be formatted according to the following diagram. The packet must always begin with the Ancillary Data Flag (ADF), defined as the following 10-bit word sequence: 000h, 3FFh, 3FFh.

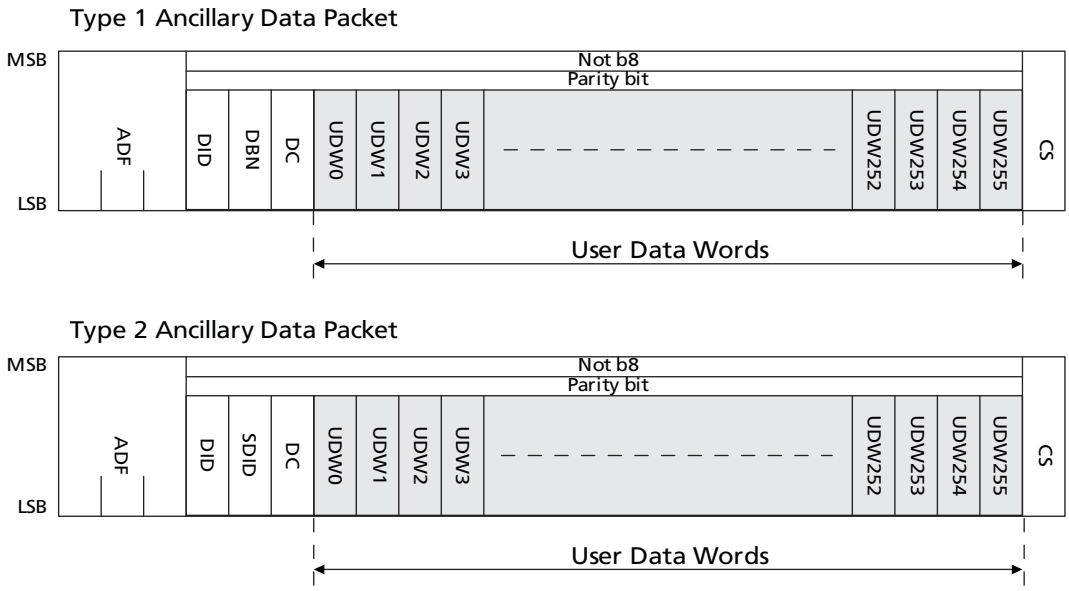


Figure 4-47: Ancillary Data Packets

The next data word is the 8-bit Data ID (DID), used to define the contents of the packet. For example, a unique DID can be used to denote alarm data, with another DID to denote status data. After the DID, there are two possible options, as shown in Figure 4-47.

A Type 1 packet defines an 8-bit Data Block Number (DBN) sequence, used to distinguish successive packets with the same DID. The DBN simply increments with each packet of the same DID, between 0 and 255.

For a Type 2 packet, an 8-bit Secondary Data ID (SDID) word is defined, which can be used to denote variants of payloads with the same DID. For example, packets with a DID to denote error data may distinguish different error types using unique SDID's.

After the DBN or SDID, the next data word is the 8-bit Data Count (DC). This word must be set to the number of user data words (UDW) that follow the DC, and must not exceed 255 (maximum payload size).

The final word of the ancillary data packet is the 9-bit Checksum (CS). The CS value must be equal to the nine least significant bits of the sum of the nine least significant bits of the DID, the DBN or the SDID, the DC and all user data words (UDW) in the packet. The CS value is automatically calculated by the GV7600.

For HD video formats, the GV7600 only inserts ancillary data packets in the Luma channel, or the DS1 presented on input pins DIN[19:10].

Horizontal or vertical ancillary data words may be inserted on up to four different lines per video frame.

Up to 512 data words may be inserted per frame with all Data Words - including the ancillary packet ADF, DBN, DCNT, DID, SDID and CSUM words - being provided by the user via host interface configuration.

The CSUM word is re-calculated and inserted by the Ancillary Data Checksum Calculation and Insertion function.

Two modes of operation are provided in ancillary insertion: Concatenated mode, and Separate Line mode.

In Concatenated mode, all 512 data words are available for insertion as either HANC or VANC packets on one line per video frame.

In Separate Line mode, up to 128 data words are available for insertion as either HANC or VANC packets on one of up to four different user programmable lines.

User configuration of the ancillary data insertion function includes the following information:

- The operating mode - Concatenated or Separate Line mode
- HANC or VANC packet type - in Single Line mode, each line may be independently identified as either VANC or HANC data. In Concatenated mode, only one ancillary packet type may be defined
- Line Number for Insertion - up to four lines may be specified in single line mode and one line in Concatenated mode
- Total number of words to insert - includes all data words for all ancillary packets to be inserted on each line
- Ancillary data - up to 512 user data words in Concatenated mode or 128 user Data Words per line in Separate Line mode

Ancillary data insertion only takes place if the PROC_EN pin is HIGH and $\overline{656\_BYPASS}$ is HIGH.

In addition, the GV7600 requires the ANC_INS bit to be set LOW in the PROC_DISABLE register.

4.8.1 Ancillary Data Insertion Operating Modes

User selection of one of the two operating modes is provided through host interface configuration, using the ANC_INS_MODE register bit. (See page 96.)

The supported operating modes are Concatenated mode and Separate Line operating mode.

By default (at power up or after system reset), the Separate Line operating mode is enabled.

Ancillary data packets are programmed into the ANC_PACKET_BANK1, ANC_PACKET_BANK2, ANC_PACKET_BANK3 & ANC_PACKET_BANK4 host registers at address 040h to 13Fh. (See page 98 and page 98.)

4.8.1.1 Separate Line Operating Mode

In Separate Line mode, it is possible to insert horizontal or vertical ancillary data on up to four lines per video frame. For each of the four video lines, up to 128 8-bit HANC or VANC data words can be inserted. Separate Line mode is selected by setting the ANC_INS_MODE bit in the host interface LOW. By default, at power up, Separate Line mode is selected.

The lines on which ancillary data is to be inserted is programmed in host register addresses 025h to 02Ch. (See page 96 to page 97.) For HD formats, the stream into which the ancillary data is to be inserted (Luma or Chroma) is also programmed in these register addresses.

The non-zero video line numbers on which to insert the ancillary data, the ancillary data type (HANC or VANC), and the total number of words to insert per line must be programmed via the host interface. (Refer to Table 4-23: Supported Video Standards for more specifics.) At power up, or after system reset, all ancillary data insertion line numbers and total number of words default to zero.

If the total number of Data Words specified per line exceeds 128 only the first 128 Data Words are inserted. The data words are programmed as two 8-bit values per address, starting at host interface address 040h in the ANC_PACKET_BANK1 register.

4.8.1.2 Concatenated Operating Mode

In Concatenated mode, it is possible to insert up to 512 8-bit horizontal or vertical ancillary Data Words on one line per video frame. Concatenated Line mode can be selected by setting the ANC_INS_MODE bit in the host interface HIGH. By default, at power up, Separate Line mode is selected.

In Concatenated mode, only the FIRST_LINE_* registers of the host interface need to be programmed (addresses 025h and 026h). See page 96.

The non-zero video line number on which to insert the ancillary data, the ancillary data type (HANC or VANC), and the total number of words to insert must be programmed via the host interface. At power up, or after system reset, the ancillary data insertion line number and total number of words default to zero.

If the total number of data words specified exceeds 512 only the first 512 Data Words are inserted. The data words are programmed as two 8-bit values per address, starting at host interface address of 040h in the ANC_PACKET_BANK1 register.

4.9 Additional Processing Functions

4.9.1 Video Format Detection

By using the timing parameters extracted from the received TRS signals, or the supplied external timing signals, the GV7600 calculates the video format.

The total samples per line, active samples per line, total lines per field/frame, and active lines per field/frame are measured and reported to the user via the four RASTER_STRUCTURE registers in the host interface.

These line and sample count registers are updated once per frame at the end of line 12.

The RASTER_STRUCTURE registers also contain two status bits: STD_LOCK and INT/$\overline{\text{PROG}}$.

The STD_LOCK bit is set HIGH whenever the automatic video format detection circuit has achieved full synchronization.

The INT/$\overline{\text{PROG}}$ bit is set LOW if the detected video standard is Progressive, and is set HIGH if the detected video standard is Interlaced.

The Gennum video standard code (VD_STD) is included in Table 4-23 for reference purposes.

Table 4-23: Supported Video Standards

Active Video Area	Length of HANC	Length of Active Video	Total Samples	Gennum VD_STD[4:0]	RATE_SEL 1
2048x1080/24 (1:1)	690	2048	2750	1Ch	1
2048x1080/25 (1:1)	580	2048	2640	1Ch	1
1920x1080/60 (1:1)	268	1920	2200	0Bh	1
1920x1080/50 (1:1)	708	1920	2640	0Dh	1
1920x1035/60 (2:1)	268	1920	2200	15h	0
1920x1080/50 (2:1)	444	1920	2376	14h	0
1920x1080/60 (2:1)	268	1920	2200	0Ah	0
1920x1080/50 (2:1)	708	1920	2640	0Ch	0
1920x1080/30 (1:1)	268	1920	2200	0Bh	0
1920x1080/25 (1:1)	708	1920	2640	0Dh	0
1920x1080/24 (1:1)	818	1920	2750	10h	0
1920x1080/25 (1:1) – EM	324	2304	2640	0Eh	0
1920x1080/24 (1:1) – EM	338	2400	2750	12h	0
1280x720/30 (1:1)	2008	1280	3300	02h	0
1280x720/30 (1:1) – EM	408	2880	3300	03h	0
1280x720/50 (1:1)	688	1280	1980	04h	0
1280x720/50 (1:1) – EM	240	1728	1980	05h	0
1280x720/25 (1:1)	2668	1280	3960	06h	0
1280x720/25 (1:1) – EM	492	3456	3960	07h	0
1280x720/24 (1:1)	2833	1280	4125	08h	0
1280x720/24 (1:1) – EM	513	3600	4125	09h	0
1280x720/60 (1:1)	358	1280	1650	00h	0
1280x720/60 (1:1) – EM	198	1440	1650	01h	0
1440x487/60 (2:1)	280	1440	1716	16h	X
1440x507/60 (2:1)	280	1440	1716	17h	X
525-line 487 generic	–	–	1716	19h	X
525-line 507 generic	–	–	1716	1Bh	X
1440x576/50 (2:1)	280	1440	1728	18h	X
625-line generic (EM)	–	–	1728	1Ah	X
RATE_SEL0 = 0 Unknown HD	–	–	–	1Dh	

Table 4-23: Supported Video Standards (Continued)

Active Video Area	Length of HANC	Length of Active Video	Total Samples	Gennum VD_STD[4:0]	RATE_SEL 1
RATE_SEL0 = 1 Unknown SD	–	–	–	1Eh	X
RATE_SEL0 = 0 Unknown Full HD	–	–	–	1Fh	1

By default (at power up or after system reset), the four RASTER_STRUCTURE, STD_LOCK and INT/$\overline{\text{PROG}}$ registers are set to zero. These registers are also cleared when the $\overline{\text{656\_BYPASS}}$ pin is LOW, or the LOCKED pin is LOW.

4.9.2 Ancillary Data Blanking

The GV7600 can blank the video input data during the H and V blanking periods. This function is enabled by setting the $\overline{\text{ANC\_BLANK}}$ pin LOW.

This function is only available when the device is operating in video mode ($\overline{\text{656\_BYPASS}}$ = HIGH).

In this mode, input video data in the horizontal and vertical blanking periods are replaced by video blanking values.

The blanking function operates only on the video input signal and removes all ancillary data already embedded in the input video stream.

In SD mode, SAV and EAV code words already embedded in the input video stream are protected and are not blanked.

In HD, SAV and EAV code words, line numbers and line based CRC's already embedded in the input video stream are protected and are not blanked.

The active image area are not blanked.

4.9.3 Ancillary Data Checksum Calculation and Insertion

The GV7600 calculates checksums for all detected ancillary data packets and audio data presented to the device.

Ancillary data checksum insertion only takes place if the PROC_EN pin is HIGH, the $\overline{\text{656\_BYPASS}}$ is HIGH and the ANC_CSUM_INS bit is set LOW in the PROC_DISABLE register.

4.9.4 TRS Generation and Insertion

The GV7600 is capable of generating and inserting TRS codes.

TRS word generation and insertion are performed in accordance with the timing parameters generated by the timing circuits, which is locked to the externally provided H:V:F or CEA-861 signals, or the TRS signals embedded in the input data stream.

10-bit TRS code words are inserted at all times.

The insertion of TRS ID words only take place if the PROC_EN pin is HIGH and the $\overline{656\_BYPASS}$ pin is HIGH.

In addition to this, the GV7600 requires the TRS_INS bit to be set LOW in the PROC_DISABLE register.

If the 861_EN pin is HIGH, then the timing circuits are locked to CEA-861 timing.

4.9.5 HD Line Number Calculation and Insertion

The GV7600 is capable of line number generation and insertion, in accordance with the relevant HD video standard, as determined by the automatic video standard detector.

Note: Line number generation and insertion only occurs in HD mode (RATE_SEL0 = LOW).

The insertion of line numbers only take place if the PROC_EN pin is HIGH and $\overline{656\_BYPASS}$ pin is HIGH.

In addition to this, the GV7600 requires the LNUM_INS bit to be set LOW in the PROC_DISABLE register.

4.9.6 Illegal Code Re-Mapping

The GV7600 detects and corrects illegal code words within the active picture area.

All codes within the active picture (outside the horizontal and vertical blanking periods), between the values of 3FCh and 3FFh are re-mapped to 3FBh. All codes within the active picture area between the values of 000h and 003h are remapped to 004h.

8-bit TRS code words and ancillary data preambles are also re-mapped to 10-bit values.

The illegal code re-mapping only takes place if the PROC_EN pin is HIGH and $\overline{656\_BYPASS}$ is HIGH.

In addition to this, the GV7600 requires the ILLEGAL_REMAP bit to be set LOW in the PROC_DISABLE register.

4.9.7 Line Based CRC Generation and Insertion

When operating in HD mode (RATE_SEL0 pin = LOW), the GV7600 generates and inserts line based CRC words into both the Y and C channels of the data stream.

The line based CRC insertion only takes place if the PROC_EN pin is HIGH and $\overline{656\_BYPASS}$ is HIGH.

In addition to this, the GV7600 requires the CRC_INS bit to be set LOW in the PROC_DISABLE register.

4.9.8 EDH Generation and Insertion

The Error Detection and Handling (EDH) concept is based on making Cyclic Redundancy Check (CRC) calculations for each field of component digital video prior to transmission over a serial digital interface, such as Aviia. Separate CRC values are calculated for the entire video field, including blanking, and the active picture region. The calculated CRC values, along with status flags, are sent with the video data over the Aviia link.

The Aviia receiver also performs the same CRC calculations and compares the values to those sent across the link. If the CRC values are not identical to the transmitted values, an error can be indicated by the receive equipment. This allows the onset of errors, systematic of faulty or poor cable and connectors, to be detected and flagged.

EDH is fully defined by a recommended practice, RP 165, from the Society of Motion Pictures and Television Engineers (SMPTE). RP 165 defines the CRC calculation ranges, error status flag handling, and format and position of the EDH packet to be embedded in the video.

The GV7600 can be configured to automatically calculate CRC values and insert EDH packets according to SMPTE RP 165. Status flags can be programmed via the host interface.

When operating in SD mode, the GV7600 generates and inserts EDH packets into the data stream.

The EDH packet generation and insertion only takes place if the PROC_EN pin is HIGH, $\overline{656\_BYPASS}$ pin is HIGH, the RATE_SEL0 pin is HIGH and the EDH_CRC_INS bit is set LOW in the PROC_DISABLE register.

Calculation of both Full Field (FF) and Active Picture (AP) CRCs is carried out by the device.

EDH error flags EDH, EDA, IDH, IDA and UES for ancillary data, full field and active picture are also inserted.

- When the EDH_CRC_UPDATE bit of the host interface is set LOW, these flags are sourced from the ANC_EDH_FLAG, FF_EDH_FLAG and AP_EDH_FLAG registers of the device, where they are programmed by the application layer.
- When the EDH_CRC_UPDATE bit of the host interface is set HIGH, incoming EDH flags are preserved and inserted in the outgoing EDH packets. In this mode the ANC_EDH_FLAG, FF_EDH_FLAG and AP_EDH_FLAG registers contain the incoming EDH flags, and are read only.

The GV7600 generates all of the required EDH packet data including all ancillary data preambles: DID, DBN, DC, reserved code words and checksum.

The prepared EDH packet is inserted at the appropriate line of the video stream (in accordance with RP165). The start pixel position of the inserted packet is based on the SAV position of that line, such that the last byte of the EDH packet (the checksum) is placed in the sample immediately preceding the start of the SAV TRS word.

Note 1: When the EDH_CRC_UPDATE bit of the host interface is set LOW, it is the responsibility of the application interface to ensure that the EDH flag registers are updated regularly (once per field).

Note 2: It is also the responsibility of the application interface to ensure that there is sufficient space in the horizontal blanking interval for the EDH packet to be inserted.

4.9.9 Video Processing

The GV7600 contains a number of signal processing features. These features are only enabled in video mode of operation ($\overline{656\_BYPASS}$ = HIGH), and when I/O processing is enabled (PROC_EN = HIGH).

Signal processing features include:

- TRS generation and insertion
- Line number calculation and insertion
- Line based CRC calculation and insertion
- Illegal code re-mapping
- Ancillary checksum calculation and correction
- EDH generation and insertion
- Audio Embedding

To enable these features in the GV7600, the $\overline{656\_BYPASS}$ pin must be HIGH, the PROC_EN pin must be HIGH and the individual feature must be enabled via bits set in the PROC_DISABLE register of the host interface. By default, all of the processing features are enabled.

4.9.10 Processing Feature Disable

The GV7600 contains a PROC_DISABLE register. This register contains one bit for each processing feature, allowing the user to enable/disable each process individually.

By default (at power up or after system reset), all of the PROC_DISABLE register bits are LOW.

To disable an individual processing feature, the application interface must set the corresponding PROC_DISABLE bit HIGH in the PROC_DISABLE register. To enable these features, the PROC_EN pin must be HIGH, and the individual feature must be enabled by setting bits LOW in the PROC_DISABLE register of the host interface.

The video processing functions supported by the GV7600 are shown in Table 4-24.

Table 4-24: PROC_DISABLE Register Bits

Video Processing Feature	PROC_DISABLE Register Bit
TRS insertion	TRS_INS (000h Bit 0)
Y and C line based CRC insertion	CRC_INS (000h Bit 2)
Y and C line number insertion	LNUM_INS (000h Bit 1)
Ancillary data checksum correction	ANC_CSUM_INS (000h Bit 3)
EDH CRC error calculation and insertion	EDH_ CRC_INS (000h Bit 4)
Illegal word re-mapping	ILLEGAL_WORD_REMAP (000h Bit 5)
Audio embedding	AUDIO_EMBED (000h Bit 10)

4.10 Parallel to Serial Conversion

The parallel data output of the internal data processing blocks is fed to the parallel to serial converter. The function of this block is to generate a serial data stream from the 20-bit or 10-bit parallel data words.

Note: The internal data path bus width may not be directly related to the parallel data bus input bus width, which is controlled by the setting of the 20BIT/$\overline{10BIT}$ pin.

4.11 Serial Clock PLL

An internal VCO provides the transmission clock rates for the GV7600.

The power supply to the VCO is provided to the VCO_VDD/VCO_GND pins of the device.

This VCO is locked to the input PCLK via an on-chip PLL and Charge Pump.

Internal division ratios for the PCLK are determined by the setting of the RATE_SEL0 pin, the RATE_SEL1 pin and the 20BIT/$\overline{10BIT}$ pin as shown in Table 4-25:

Table 4-25: PCLK and Serial Digital Clock Rates

External Pin Setting			Supplied PCLK Rate	Serial Digital Output Rate
RATE_SEL0	RATE_SEL1	20BIT/$\overline{10BIT}$		
LOW	HIGH	HIGH	148.5 or 148.5/1.001MHz	2.97 or 2.97/1.001 Gb/s
LOW	HIGH	LOW	148.5 or 148.5/1.001MHz (DDR)	2.97 or 2.97/1.001 Gb/s
LOW	LOW	HIGH	74.25 or 74.25/1.001MHz	148.5 or 148.5/1.001Gb/s
LOW	LOW	LOW	148.5 or 148.5/1.001MHz	148.5 or 148.5/1.001Gb/s
HIGH	LOW	HIGH	13.5MHz	270Mb/s
HIGH	LOW	LOW	27MHz	270Mb/s

As well as generating the serial digital output clock signals, the PLL is also responsible for generating all internal clock signals required by the device.

4.11.1 PLL Bandwidth

Table 4-26 shows the GV7600 PLL loop bandwidth variations. PLL bandwidth is a function of the external loop filter resistor and the charge pump current. We recommend using a 200Ω loop filter resistor, however, this value can be varied from 100Ω to 380Ω, depending on application. Values other than 200Ω are not guaranteed. As the resistor is changed, the bandwidth scales proportionately (for example, a change from a 200Ω to 300Ω resistor causes a 50% increase in bandwidth). The charge pump current is preset to 100µA and should not be changed. The

external loop filter capacitors do not impact the PLL bandwidth. The external loop filter capacitors affect PLL loop settling time, phase margin and noise.

Table 4-26: GV7600 PLL Bandwidth

Mode	PCLK Frequency (MHz)	Filter Resistor (Ω)	Charge Pump Current (μA)	Bandwidth (kHz)
SD	13.50	200	100	4.78
SD	27.00	200	100	9.57
HD	74.25	200	100	26.32
HD	148.50	200	100	52.63
Full HD	148.50	200	100	52.63

4.12 Lock Detect

The Lock Detect block controls the serial digital output signal and indicates to the application layer the lock status of the device.

The LOCKED output pin is provided to indicate the device operating status.

The LOCKED output signal is set HIGH by the lock detect block under the following conditions (see Table 4-27):

Table 4-27: GV7600 Lock Detect Indication

$\overline{\text{RESET}}$	PLL Lock	$\overline{\text{656\_BYPASS}}$	ASI	RATE_SEL 0
HIGH	HIGH	HIGH	LOW	X
HIGH	HIGH	LOW	HIGH	HIGH
HIGH	HIGH	LOW	LOW	X

Any other combination of signal states not included in Table 4-27 results in the LOCKED pin being LOW.

Note: When the LOCKED pin is LOW, the serial digital output is in the muted state.

4.13 Serial Digital Output

The GV7600 has a single, low-impedance current mode differential output driver, capable of driving at least 800mV into a 75Ω single-ended load.

The output signal amplitude, or swing, are user-configurable using an external resistor on the RSET pin.

The SDO and $\overline{\text{SDO}}$ pins of the device provide the serial digital output.

Compliance with all requirements defined in Section 4.13.1 through Section 4.13.3 is guaranteed when measured across a 75Ω terminated load at the output of 1m of Belden 1694A cable, including the effects of the Gennum recommended ORL matching network, BNC and coaxial cable connection, except where otherwise stated.

Figure 4-48 illustrates this requirement.

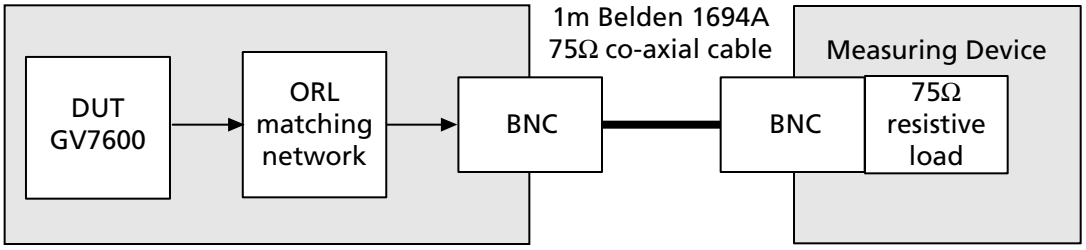


Figure 4-48: ORL Matching Network, BNC and Coaxial Cable Connection

4.13.1 Output Signal Interface Levels

The Serial Digital Output signals (SDO and $\overline{\text{SDO}}$ pins), of the device meet the amplitude requirements as defined in ITU-R BT.656 and BT.1120 for an unbalanced generator (single-ended).

The signal amplitude is controlled to better than +/-7% of the nominal level, when an external 750Ω 1% resistor is connected between the RSET pin of the device and VCC.

The output signal amplitude can be reduced to less than 1/10th of the nominal amplitude, defined above, by increasing the value of the resistor connected between the RSET pin of the device and VCC.

These requirements are met across all ambient temperature and power supply operating conditions described in 2. Electrical Characteristics.

The output amplitude of the GV7600 can be adjusted by changing the value of the RSET resistor as shown in Table 4-28. For a 800mVp-p output a value of 750Ω is required. A ±1% SMT resistor should be used.

The RSET resistor is part of the high speed output circuit of the GV7600. The resistor should be placed as close as possible to the RSET pin. In addition, an anti-pad should be used underneath the resistor.

Table 4-28: R_{SET} Resistor Value vs. Output Swing

R_{SET} Resistor Values (Ω)	Output Swing (mV_{p-p})
995	608
824	734
750	800
680	884

4.13.2 Slew Rate Selection

The GV7600 supports two user-selectable output slew rates.

Control of the slew rate is determined by the setting of the RATE_SEL0 input pin.

When this pin is set HIGH, the output slew rate matches the requirements as defined by the ITU-R BT.656 standard.

When this pin is set LOW, the output slew rate is better than the requirements as defined by the ITU-R BT.1120 standard.

These requirements is met across all ambient temperature and power supply operating conditions described in the 2. Electrical Characteristics.

This requirement is summarized in Table 4-29:

Table 4-29: Serial Digital Output - Rise/Fall Time

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Serial Output Rise/Fall Time 20% ~ 80%	SDO_{TR}	HD signal	–	–	135	ps
		SD signal	400	–	800	ps

4.13.3 Serial Digital Output Mute

When the SDO_EN pin is LOW, the serial digital output signals of the device become high-impedance, reducing system power.

The serial digital output is also placed in the high-impedance state when the LOCKED pin is LOW, or when the STANDBY pin is HIGH.

4.14 Gennum Serial Peripheral Interface

The GSPI, or Gennum Serial Peripheral Interface, is a 4-wire interface provided to allow the application layer to access additional status information through configuration registers in the GV7600.

The GSPI comprises a Serial Data Input signal (SDIN), Serial Data Output signal (SDOUT), an active low Chip Select ($\overline{CS}$) and a Burst Clock (SCLK).

The SCLK, SDIN and $\overline{CS}$ signals are provided by the application interface. The SDOUT pin is a non-clocked loop-through of SDIN, and may be connected to the SDIN of another device, allowing multiple devices to be connected to the GSPI chain. The interface is illustrated in Figure 4-49 below.

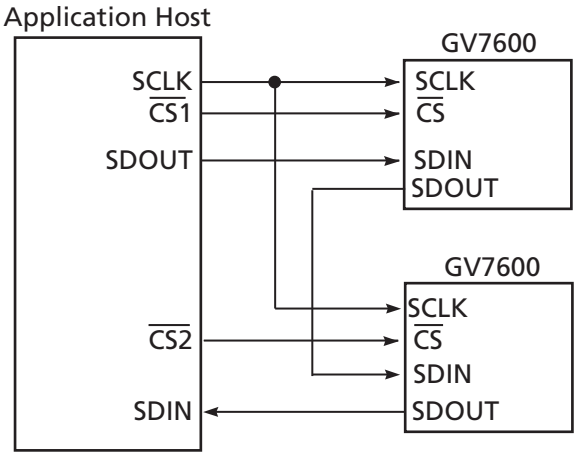


Figure 4-49: GSPI Application Interface Connection

All read or write access to the GV7600 is initiated and terminated by the application host processor. Each access always begins with a Command/Address Word followed by a data read or write.

4.14.1 Command Word Description

The Command Word consists of a 16-bit word transmitted MSB first and contains a read/write bit, an Auto-Increment bit and a 12-bit address. Figure 4-50 shows the command word format and bit configurations.

Command Words are clocked into the GV7600 on the rising edge of the Serial Clock SCLK, which operates in a burst fashion.

When the Auto-Increment bit is set LOW, each Command Word must be followed by only one Data Word to ensure proper operation. If the Auto-Increment bit is set HIGH, the following Data Word is written into the address specified in the Command Word, and subsequent data words are written into incremental addresses from the previous Data Word. This facilitates multiple address writes without sending a Command Word for each Data Word.

Note: All registers can be written to through single address access or through the Auto-increment feature. However, the LSB of the video registers cannot be read through

single address read-back. Single address read-back returns a zero value for the LSB. If auto-increment is used to read back the values from at least two registers, the LSB value read is always correct. Therefore, for register read-back, it is recommended that auto-increment be used and that at least two registers be read back at a time.

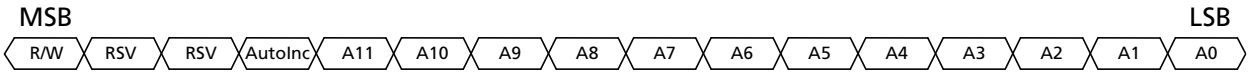


Figure 4-50: Command Word Format

4.14.2 Data Read or Write Access

Serial data is transmitted or received MSB first synchronous with the rising edge of the Serial Clock, SCLK. The Chip Select ($\overline{CS}$) signal must be active LOW a minimum of 1.5ns (t_0 in Figure 4-52) before the first clock edge to ensure proper operation.

During a Read sequence (Command Word R/W bit set HIGH), a wait state of 148ns (4 x $1/f_{PCLK}$, t_5 in Figure 4-52) is required between writing the Command Word and reading the following Data Word. The read bits are clocked out on the negative edges of SCLK.

Note 1: Where several devices are connected to the GSPI chain, only one $\overline{CS}$ may be asserted during a read sequence.

During a Write sequence (Command Word R/W bit set LOW), a wait state of 37ns (1 x $1/f_{PCLK}$, t_4 in Figure 4-52) is required between the Command Word and the following Data Word. This wait state must also be maintained between successive Command Word/Data Word write sequences. When Auto-increment mode is selected (AutoInc = 1), the wait state must be maintained between successive Data Words after the initial Command Word/Data Word sequence.

During the write sequence, all command and following Data Words input at the SDIN pin are output at the SDOUT pin as is.

When several devices are connected to the GSPI chain, data can be written simultaneously to all the devices which have $\overline{CS}$ set LOW.

Note 2: If the application interface performs a Read or Write access after power-up, prior to the application of a valid serial video input signal, the SCLK frequency must not exceed 10MHz.

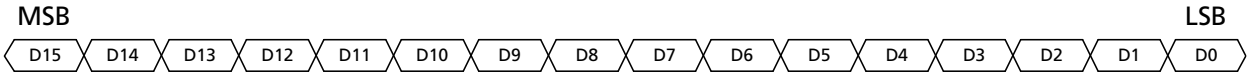


Figure 4-51: Data Word Format

4.14.3 GSPI Timing

Write and Read Mode timing for the GSPI interface is as shown in the following diagrams:

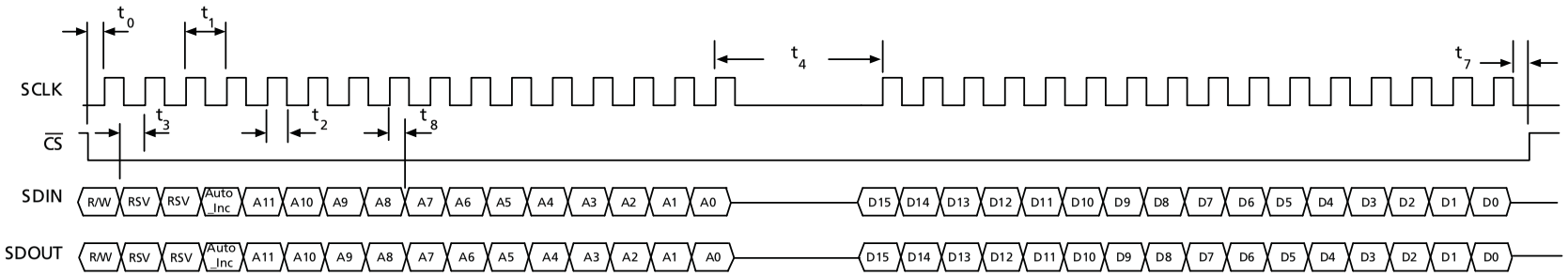


Figure 4-52: Write Mode

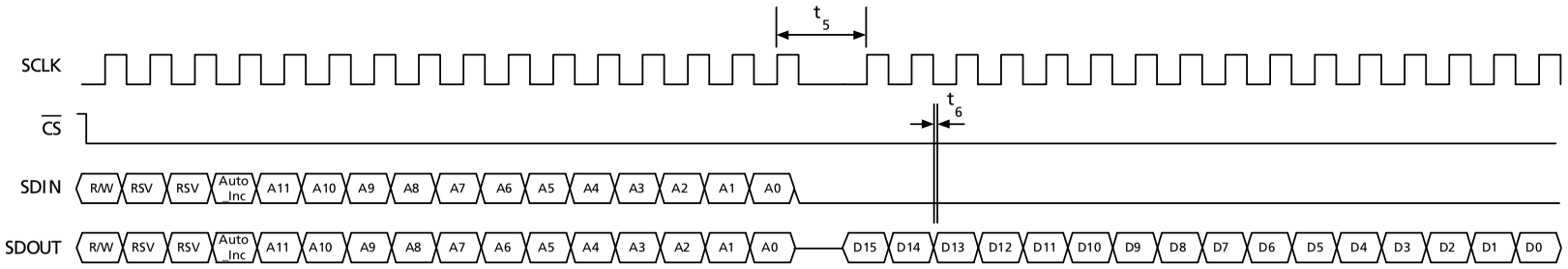


Figure 4-53: Read Mode

4.14.3.1 GSPI Timing Delays

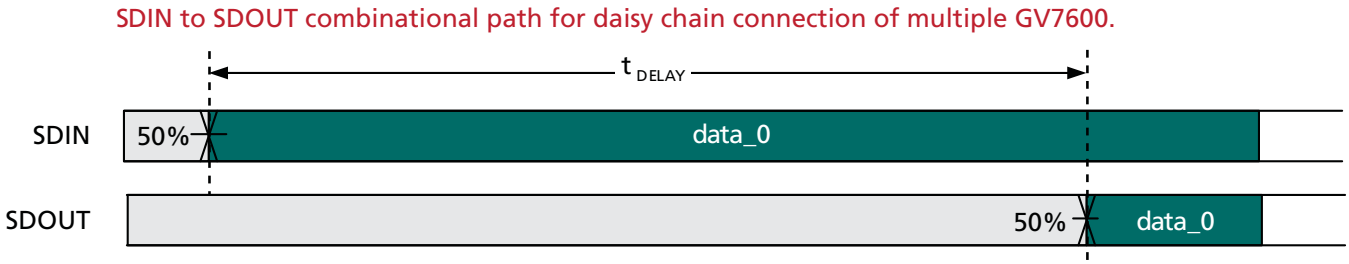


Figure 4-54: GV7600 GSPI Timing Delays

Table 4-30: GV7600 GSPI Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input data delay time	t_{DELAY}	50% levels; 1.8V operation	–	–	10.5	ns
Input data delay time	t_{DELAY}	50% levels; 3.3V operation	–	–	8.7	ns

4.15 Host Interface Register Maps

4.15.1 Video Core Registers

Table 4-29: Video Core Configuration and Status Registers

Address	Register Bit Name	Bit	Description	R/W	Default
000h	RSVD	15-13	Reserved.	R/W	0
	EDH_CRC_UPDATE	12	HIGH = preserve incoming EDH flags and insert into outgoing EDH packets. LOW = embed flags from 003h in EDH packet.	R/W	0
	ANC_INS	11	HIGH = disable ancillary data insertion. LOW = embeds ancillary data packet stored at 040h to 013h according to parameters at 005h to 02Dh.	R/W	0
	AUDIO_EMBED	10	HIGH = disable audio embedding. LOW = enables audio embedding.	R/W	0
	RSVD	9	Reserved.	R/W	1
	H_CONFIG	8	Chooses H configuration: HIGH = TRS based H timing. LOW = Active Picture timing.	R/W	0
	RSVD	7-6	Reserved.	R/W	0
	ILLEGAL_WORD_REMAP	5	HIGH = disables illegal word remapping.	R/W	0
	EDH_CRC_INS	4	HIGH = disables EDH CRC error correction and insertion.	R/W	0
	ANC_CSUM_INS	3	HIGH = disables insertion of ancillary data checksums.	R/W	0
	CRC_INS	2	HIGH = disables insertion of HD CRC words.	R/W	0
	LNUM_INS	1	HIGH = disables insertion of HD line numbers.	R/W	0
	TRS_INS	0	HIGH = disables insertion of TRS words.	R/W	0

Table 4-29: Video Core Configuration and Status Registers (Continued)

Address	Register Bit Name	Bit	Description	R/W	Default
001h	RSVD	15-7	Reserved.	R	0
	TRS_PERR	6	TRS protection error. HIGH = Errors in TRS. LOW = No errors in TRS.	R	0
	Y1_EDH_CS_ERR	5	Same as CS_ERR but only updates its state when packet being inspected is an EDH packet.	R	0
	Y1_CS_ERR	4	HIGH indicates that a checksum error is detected. It is updated every time a $\overline{CS}$ word is present on the output.	R	0
	FORMAT_ERR	3	HIGH indicates standard is not recognized for 861D conversion.	R	0
	RSVD	2-1	Reserved.	R	0
001h	LOCK_ERR	0	HIGH indicates PLL lock error indication.	R	0
002h	RSVD	15	Reserved.	R	0
	ANC_UES_EXT	14	Ancillary data - unknown error status flag.	R	0
	ANC_IDA_EXT	13	Ancillary data - internal error detected already flag.	R	0
	ANC_IDH_EXT	12	Ancillary data - internal error detected here flag.	R	0
	ANC_EDA_EXT	11	Ancillary data - error detected already flag.	R	0
	ANC_EDH_EXT	10	Ancillary data - error detected here flag.	R	0
	FF_UES_EXT	9	EDH Full Field - unknown error status flag.	R	0
	FF_IDA_EXT	8	EDH Full Field - internal error detected already flag.	R	0
	FF_IDH_EXT	7	EDH Full Field - internal error detected here flag.	R	0
	FF_EDA_EXT	6	EDH Full Field - error detected already flag.	R	0
	FF_EDH_EXT	5	EDH Full Field - error detected here flag.	R	0
	AP_UES_EXT	4	EDH Active Picture - unknown error status flag.	R	0
	AP_IDA_EXT	3	EDH Active Picture - internal error detected already flag.	R	0
	AP_IDH_EXT	2	EDH Active Picture - internal error detected here flag.	R	0
	AP_EDA_EXT	1	EDH Active Picture - error detected already flag.	R	0
	AP_EDH_EXT	0	EDH Active Picture - error detected here flag.	R	0

Table 4-29: Video Core Configuration and Status Registers (Continued)

Address	Register Bit Name	Bit	Description	R/W	Default
003h	RSVD	15	Reserved.	R	0
	ANC_UES_PGM	14	Ancillary data - unknown error status flag.	R/W	0
	ANC_IDA_PGM	13	Ancillary data - internal error detected already flag.	R/W	0
	ANC_IDH_PGM	12	Ancillary data - internal error detected here flag.	R/W	0
	ANC_EDA_PGM	11	Ancillary data - error detected already flag.	R/W	0
	ANC_EDH_PGM	10	Ancillary data - error detected here flag.	R/W	0
	FF_UES_PGM	9	EDH Full Field - unknown error status flag.	R/W	0
	FF_IDA_PGM	8	EDH Full Field - internal error detected already flag.	R/W	0
	FF_IDH_PGM	7	EDH Full Field - internal error detected here flag.	R/W	0
	FF_EDA_PGM	6	EDH Full Field - error detected already flag.	R/W	0
	FF_EDH_PGM	5	EDH Full Field - error detected here flag.	R/W	0
	AP_UES_PGM	4	EDH Active Picture - unknown error status flag.	R/W	0
	AP_IDA_PGM	3	EDH Active Picture - internal error detected already flag.	R/W	0
	AP_IDH_PGM	2	EDH Active Picture - internal error detected here flag.	R/W	0
003h	AP_EDA_PGM	1	EDH Active Picture - error detected already flag.	R/W	0
	AP_EDH_PGM	0	EDH Active Picture - error detected here flag.	R/W	0
004h	RSVD	15-10	Reserved.	R	0
	VD_STD	9-5	Detected video standard.	R	0
	INT/$\overline{\text{PROGB}}$	4	HIGH = interlaced signal LOW = progressive signal	R	0
	RSVD	3	Reserved.	R	0
	SRD_LOCK	2	Standard lock indication. Active HIGH.	R	0
	V_LOCK	1	Vertical lock indication. Active HIGH.	R	0
	H_LOCK	0	Horizontal lock indication. Active HIGH.	R	0
005h	RSVD	15-0	Reserved.	R	1027
006h	RSVD	15-0	Reserved.	R	0
007h	RSVD	15-2	Reserved.	R	0
	FF_CRC_V	1	Full Field extracted V bit.	R	0
	AP_CRC_V	0	Active Picture extracted V bit.	R	0
008h	RSVD	15-0	Reserved.	R	1
009h to 011h	RSVD	–	Reserved.	R/W	0

Table 4-29: Video Core Configuration and Status Registers (Continued)

Address	Register Bit Name	Bit	Description	R/W	Default
012h	RSVD	15-11	Reserved.	R	0
	LINES_PER_FRAME	10-0	Total lines per frame.	R	0
013h	RSVD	15-14	Reserved.	R	0
	WORDS_PER_LINE	13-0	Total words per line.	R	0
014h	RSVD	15-13	Reserved.	R	0
	ACTIVE_WORDS_PER_LINE	12-0	Words per active line.	R	0
015h	RSVD	15-11	Reserved.	R	0
	ACTIVE_LINES_PER_FIELD	10-0	Active lines per frame.	R	0
016h to 023h	RSVD	–	Reserved.	R	0
024h	RSVD	15-2	Reserved.	R	0
	PACKET_MISSED	1	Ancillary data packet could not be inserted in its entirety. HIGH = Ancillary data packet cannot be inserted in its entirety.	R	0
	RW_CONFLICT	0	Same RAM address was read and written to at the same time. HIGH = one of the addressed from 040h to 13Fh was read and written to at the same time.	R	0
025h	RSVD	15-12	Reserved.	R	0
	ANC_INS_MODE	11	Ancillary data insertion mode. HIGH = Concatenate LOW = Separate	R/W	0
	FIRST_LINE_NUMBER	10-0	First line number to insert ancillary packet on.	R/W	0
026h	FIRST_LINE_NUMBER_ANC_TYPE	15	Ancillary region to insert packet in. HIGH = VANC. LOW = HANC.	R/W	0
	FIRST_LINE_NUMBER_STREAM_TYPE	14	Stream to insert packet in HIGH = C stream. LOW = Y stream.	R/W	0
	RSVD	13-10	Reserved.	R	0
	FIRST_LINE_NUMBER_OF_WORDS	9-0	Total number of words in ancillary packet to be inserted.	R/W	0
027h	RSVD	15-11	Reserved.	R	0
	SECOND_LINE_NUMBER	10-0	Second line number to insert ancillary packet on in Separate Line mode.	R/W	0

Table 4-29: Video Core Configuration and Status Registers (Continued)

Address	Register Bit Name	Bit	Description	R/W	Default
028h	SECOND_LINE_NUMBER _ANC_TYPE	15	Ancillary region to insert packet in. HIGH = VANC. LOW = HANC.	R/W	0
	SECOND_LINE_NUMBER _STREAM_TYPE	14	Stream to insert packet in. HIGH = C stream. LOW = Y stream.	R/W	0
	RSVD	13-10	Reserved.	R	0
	SECOND_LINE_NUMBER _OF_WORDS	9-0	Total number of words in ancillary packet to be inserted.	R/W	0
029h	RSVD	15-11	Reserved.	R	0
	THIRD_LINE_NUMBER	10-0	Third line number to insert ancillary packet on in Separate Line mode.	R/W	0
02Ah	THIRD_LINE_NUMBER _ANC_TYPE	15	Ancillary region to insert packet in. HIGH = VANC. LOW = HANC.	R/W	0
	THIRD_LINE_NUMBER _STREAM_TYPE	14	Stream to insert packet in. HIGH = C stream. LOW = Y stream.	R/W	0
	RSVD	13-10	Reserved.	R	0
	THIRD_LINE_NUMBER _OF_WORDS	9-0	Total number of words in ancillary packet to be inserted.	R/W	0
02Bh	RSVD	15-11	Reserved.	R	0
	FOURTH_LINE_NUMBER	10-0	Fourth line number to insert ancillary packet on in Seperate Line mode.	R/W	0
02Ch	FOURTH_LINE_NUMBER _ANC_TYPE	15	Ancillary region to insert packet in. HIGH = VANC. LOW= HANC.	R/W	0
	FOURTH_LINE_NUMBER _STREAM_TYPE	14	Stream to insert packet in. HIGH = C stream. LOW = Y stream.	R/W	0
	RSVD	13-10	Reserved.	R	0
	FOURTH_LINE_NUMBER _OF_WORDS	9-0	Total number of words in ancillary packet to be inserted.	R/W	0

Table 4-29: Video Core Configuration and Status Registers (Continued)

Address	Register Bit Name	Bit	Description	R/W	Default
02Dh	RSVD	15-5	Reserved.	R	0
	EDH_LINE_CHECK_EN	4	HIGH = ancillary block does not insert data into the EDH region of the HANC space. LOW = ancillary block inserts data into the EDH region.	R/W	1
	RSVD	3-0	Reserved.	R/W	0
02Eh to 03Fh	RSVD	–	Reserved.	R	0
040h to 07Fh	ANC_PACKET_BANK1	15-0	First bank of user defined 8-bit ancillary data. Bit 15-8: Second byte (MSB to LSB) Bit 7-0: First byte (MSB to LSB) See 4.8.1 Ancillary Data Insertion Operating Modes for details.	R/W	
080h to 0BFh	ANC_PACKET_BANK2	15-0	Second bank of user defined 8-bit ancillary data. Bit 15-8: Second byte (MSB to LSB) Bit 7-0: First byte (MSB to LSB) See 4.8.1 Ancillary Data Insertion Operating Modes for details.	R/W	
0C0h to 0FFh	ANC_PACKET_BANK3	15-0	Third bank of user defined 8-bit ancillary data. Bit 15-8: Second byte (MSB to LSB) Bit 7-0: First byte (MSB to LSB) See 4.8.1 Ancillary Data Insertion Operating Modes for details.	R/W	
100h to 13Fh	ANC_PACKET_BANK4	15-0	Fourth bank of user defined 8-bit ancillary data. Bit 15-8: Second byte (MSB to LSB) Bit 7-0: First byte (MSB to LSB) See 4.8.1 Ancillary Data Insertion Operating Modes for details.	R/W	
140h to 20Dh	RSVD	–	Reserved.	R	0

Table 4-29: Video Core Configuration and Status Registers (Continued)

Address	Register Bit Name	Bit	Description	R/W	Default
20Eh	RSVD	15-6	Reserved.	R/W	0
	AUDIO_INT_DS	5-4	Drive strength value for AUDIO_INT pin. 00 = 4mA; 01 = 6mA; 10 = 8mA(1.8V), 10mA(3.3V); 11 = 10mA(1.8V), 12mA(3.3V)	R/W	0
	LOCKED_DS	3-2	Drive strength value for LOCKED pin. 00 = 4mA; 01 = 6mA; 10 = 8mA(1.8V), 10mA(3.3V); 11 = 10mA(1.8V), 12mA(3.3V)	R/W	0
	SDOUT_TDO_DS	1-0	Drive strength value for SDOUT_TDO pin. 00 = 4mA; 01 = 6mA; 10 = 8mA(1.8V), 10mA(3.3V); 11 = 10mA(1.8V), 12mA(3.3V)	R/W	2
20Fh	RSVD	15-0	Reserved.	R/W	0
210h	TDO_DS	15-14	Drive strength value for TDO pin. 00 = 4mA; 01 = 6mA; 10 = 8mA(1.8V), 10mA(3.3V); 11 = 10mA(1.8V), 12mA(3.3V)	R/W	0
	RSVD	13-0	Reserved.	R/W	0
211h to 232h	RSVD	15-0	Reserved.	R	0

4.16 SD Audio Core

Table 4-30: SD Audio Core Configuration and Status Registers

Address	Register Name	Bit	Description	R/W	Default
400h	CTR_AGR	15	Selects replacement of audio control packets. HIGH = Replace all audio control packets LOW = Do not replace audio control packets	R/W	0
	AGR	14	Selects Audio Group Replacement operating mode.	R/W	0
	ONE_AGR	13	Specifies the replacement of just the primary group. HIGH = Replace only the primary group. LOW = Replace both the primary and secondary groups.	R/W	0
	CTRB_ON	12	Specifies the embedding of the secondary group audio control packets. Active HIGH.	R/W	1
	CLEAR_AUDIO	11	Clears all audio FIFO buffers and puts them in the start-up state. Active HIGH	R/W	0
	AFNB_AUTO	10	Enables Secondary group audio frame number generation. Active HIGH.	R/W	1
	CTRA_ON	9	Specifies the embedding of primary group audio control packets. Active HIGH.	R/W	1
	AUDIO_24BIT	8	Specifies the sample size for embedded audio. HIGH = 24-bit LOW = 20-bit / 16-bit	R/W	0
	AFNA_AUTO	7	Enables Primary group audio frame number generation. Active HIGH.	R/W	1
	AFN_OFS	6-4	Offset to add to generated Audio Frame Number. Must be in the range of 0 to 4.	R/W	0
	IDB	3-2	Specifies the primary audio group to embed. **Note**: Should IDA and IDB be set to the same value, they automatically revert to their default values.	R/W	1
	IDA	1-0	Specifies the secondary audio group to embed. **Note**: Should IDA and IDB be set to the same value, they automatically revert to their default values.	R/W	0
401h	RSVD	15-0	Reserved.	R	0

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
402h	RSVD	15-4	Reserved.	R	0
	AES_ERRD	3	Stereo Pair D audio input parity error when using AES format. Automatically cleared when read.	R	0
	AES_ERRC	2	Stereo Pair C audio input parity error when using AES format. Automatically cleared when read.	R	0
	AES_ERRB	1	Stereo Pair B audio input parity error when using AES format. Automatically cleared when read.	R	0
	AES_ERRA	0	Stereo Pair A audio input parity error when using AES format. Automatically cleared when read.	R	0
403h	RSVD	15-1	Reserved.	R	0
	ACS_REGEN	0	Specifies that Audio Channel Status of all channels should be replaced with ACSR[183:0] field. LOW = Do not replace Channel Status. HIGH = Replace Channel Status of all channels.	R/W	0
404h	RSVD	15-14	Reserved.	R	0
	AXPG4_DET	13	Set while Group 4 audio extended packets are detected.	R	0
	AXPG3_DET	12	Set while Group 3 audio extended packets are detected.	R	0
	AXPG2_DET	11	Set while Group 2 audio extended packets are detected.	R	0
	AXPG1_DET	10	Set while Group 1 audio extended packets are detected.	R	0
	ACPG4_DET	9	Set while Group 4 audio control packets are detected.	R	0
	ACPG3_DET	8	Set while Group 3 audio control packets are detected.	R	0
	ACPG2_DET	7	Set while Group 2 audio control packets are detected.	R	0
	ACPG1_DET	6	Set while Group 1 audio control packets are detected.	R	0
	ADPG4_DET	5	Set while Group 4 audio data packets are detected.	R	0
	ADPG3_DET	4	Set while Group 3 audio data packets are detected.	R	0
	ADPG2_DET	3	Set while Group 2 audio data packets are detected.	R	0
	ADPG1_DET	2	Set while Group 1 audio data packets are detected.	R	0
	ACS_APPLY_WAITB	1	Set while the GV7600 is waiting for a status boundary in the Secondary group before applying the ACSR[183:0] data to that group.	R	0
	ACS_APPLY_WAITA	0	ACS_APPLY_WAITA: Set while the GV7600 is waiting for a status boundary in Primary group before applying the ACSR[183:0] data.	R	0

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
405h	RSVD	15-0	Reserved.	R	0
406h	RSVD	15-1	Reserved.	R	0
	EN_CASCADE	0	If HIGH, puts the GV7600 into cascade mode. This bit is only effective if the AGR bit = LOW.	R/W	0
407h to 40Ah	RSVD	-	Reserved.	R	0
40Bh	AMD	15-14	Audio input format selector for Stereo Pair D input channels 7 and 8. 00 = AES/EBU or S/PDIF 01 = Serial Left Justified, MSB First 10 = Serial Right Justified, MSB First 11 = I^2S (Default)	R/W	3
	AMC	13-12	Audio input format selector for Stereo Pair C input channels 5 and 6. (See above for decoding.)	R/W	3
	AMB	11-10	Audio input format selector for Stereo Pair B input channels 3 and 4. (See above for decoding.)	R/W	3
	AMA	9-8	Audio input format selector for Stereo Pair A input channels 1 and 2. (See above for decoding.)	R/W	3
	MUTE8	7	Audio input channel 8 mute enable. Active HIGH.	R/W	0
	MUTE7	6	Audio input channel 7 mute enable. Active HIGH.	R/W	0
	MUTE6	5	Audio input channel 6 mute enable. Active HIGH.	R/W	0
	MUTE5	4	Audio input channel 5 mute enable. Active HIGH.	R/W	0
	MUTE4	3	Audio input channel 4 mute enable. Active HIGH.	R/W	0
	MUTE3	2	Audio input channel 3 mute enable. Active HIGH.	R/W	0
	MUTE2	1	Audio input channel 2 mute enable. Active HIGH.	R/W	0
	MUTE1	0	Audio input channel 1 mute enable. Active HIGH.	R/W	0

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
40Ch	RSVD	15	Reserved.	R	0
	GPA_WCLK_SRC	14-12	Primary Audio group word clock source selector. Input channel 1 = 000 Input channel 2 = 001 Input channel 3 = 010 Input channel 4 = 011 Input channel 5 = 100 Input channel 6 = 101 Input channel 7 = 110 Input channel 8 = 111	R/W	0
	GPA_CH4_SRC	11-9	Primary Audio group channel 4 source selector. 011.	R/W	3
	GPA_CH3_SRC	8-6	Primary Audio group channel 3 source selector. 010.	R/W	2
	GPA_CH2_SRC	5-3	Primary Audio group channel 2 source selector. 001.	R/W	1
40Ch	GPA_CH1_SRC	2-0	Primary Audio group channel 1 source selector. 000 = Input channel.	R/W	0
40Dh	RSVD	15	Reserved.	R	0
	GPB_WCLK_SRC	14-12	Secondary Audio group word clock source selector.	R/W	4
	GPB_CH4_SRC	11-9	Secondary Audio group channel 4 source selector.	R/W	7
	GPB_CH3_SRC	8-6	Secondary Audio group channel 3 source selector.	R/W	6
	GPB_CH2_SRC	5-3	Secondary Audio group channel 2 source selector.	R/W	5
	GPB_CH1_SRC	2-0	Secondary Audio group channel 1 source selector.	R/W	4

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
40Eh	RSVD	15	Reserved.	R/W	0
	EN_NO_VIDEO	14	Mask bit when the video format is unknown.	R/W	0
	RSVD	13-12	Reserved.	R/W	0
	EN_AES_ERRD	11	Asserts AUDIO_INT when the AES_ERRD flag is set.	R/W	0
	EN_AES_ERRC	10	Asserts AUDIO_INT when the AES_ERRC flag is set.	R/W	0
	EN_AES_ERRB	9	Asserts AUDIO_INT when the AES_ERRB flag is set.	R/W	0
	EN_AES_ERRA	8	Asserts AUDIO_INT when the AES_ERRA flag is set.	R/W	0
	EN_ACPG4_DET	7	Asserts AUDIO_INT when the ACPG4_DET flag is set.	R/W	0
	EN_ACPG3_DET	6	Asserts AUDIO_INT when the ACPG3_DET flag is set.	R/W	0
	EN_ACPG2_DET	5	Asserts AUDIO_INT when the ACPG2_DET flag is set.	R/W	0
	EN_ACPG1_DET	4	Asserts AUDIO_INT when the ACPG1_DET flag is set.	R/W	0
	EN_ADPG4_DET	3	Asserts AUDIO_INT when the ADPG4_DET flag is set.	R/W	0
	EN_ADPG3_DET	2	Asserts AUDIO_INT when the ADPG3_DET flag is set.	R/W	0
	EN_ADPG2_DET	1	Asserts AUDIO_INT when the ADPG2_DET flag is set.	R/W	0
	EN_ADPG1_DET	0	Asserts AUDIO_INT when the ADPG1_DET flag is set.	R/W	0
40Fh	RSVD	15-13	Reserved.	R	0
	MUTE_ALL	12	Mutes all input audio channels.	R/W	0
	LSB_FIRSTD	11	Causes the fourth stereo pair serial input formats to use LSB first. Used in conjunction with AMD, and only relevant when AMD is 01 or 10, Figure 4-42 to Figure 4-45.	R/W	0
	LSB_FIRSTC	10	Causes the third stereo pair serial input formats to use LSB first. Used in conjunction with AMD, and only relevant when AMD is 01 or 10, Figure 4-42 to Figure 4-45.	R/W	0
	LSB_FIRSTB	9	Causes the second stereo pair serial input formats to use LSB first.Used in conjunction with AMD, and only relevant when AMD is 01 or 10, Figure 4-42 to Figure 4-45.	R/W	0

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
40Fh	LSB_FIRSTA	8	Causes the first stereo pair serial input formats to use LSB first. Used in conjunction with AMD, and only relevant when AMD is 01 or 10, Figure 4-42 to Figure 4-45.	R/W	0
	ACT8	7	Specifies embedding of secondary audio group channel 8. Active HIGH.	R/W	1
	ACT7	6	Specifies embedding of secondary audio group channel 7. Active HIGH.	R/W	1
	ACT6	5	Specifies embedding of secondary audio group channel 6. Active HIGH.	R/W	1
	ACT5	4	Specifies embedding of secondary audio group channel 5. Active HIGH.	R/W	1
	ACT4	3	Specifies embedding of primary audio group channel 4. Active HIGH.	R/W	1
	ACT3	2	Specifies embedding of primary audio group channel 3. Active HIGH.	R/W	1
	ACT2	1	Specifies embedding of primary audio group channel 2. Active HIGH.	R/W	1
	ACT1	0	Specifies embedding of primary audio group channel 1. Active HIGH.	R/W	1
410h	RSVD	15-1	Reserved.	R	0
	XPOINT_ERROR	0	Set when the crosspoint switch is configured to put the same audio channel in both Primary and Secondary Groups.	R	0
411h to 41Fh	RSVD	–	Reserved.	R	0
420h	RSVD	15-8	Reserved.	R	0
	ACSR_BYTE_1	7-0	Audio channel status block byte 1.	R/W	133
421h	RSVD	15-8	Reserved.	R	0
	ACSR_BYTE_2	7-0	Audio channel status block byte 2.	R/W	8
422h	ACSR_BYTE_4	15-8	Audio channel status block byte 4.	R/W	0
	ACSR_BYTE_3	7-0	Audio channel status block byte 3.	R/W	44
423h	ACSR_BYTE_6	15-8	Audio channel status block byte 6.	R/W	0
	ACSR_BYTE_5	7-0	Audio channel status block byte 5.	R/W	0
424h	ACSR_BYTE_8	15-8	Audio channel status block byte 8.	R/W	0
	ACSR_BYTE_7	7-0	Audio channel status block byte 7.	R/W	0

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
425h	ACSR_BYTE_10	15-8	Audio channel status block byte 10.	R/W	0
	ACSR_BYTE_9	7-0	Audio channel status block byte 9.	R/W	0
426h	ACSR_BYTE_12	15-8	Audio channel status block byte 12.	R/W	0
	ACSR_BYTE_11	7-0	Audio channel status block byte 11.	R/W	0
427h	ACSR_BYTE_14	15-8	Audio channel status block byte 14.	R/W	0
	ACSR_BYTE_13	7-0	Audio channel status block byte 13.	R/W	0
428h	ACSR_BYTE_16	15-8	Audio channel status block byte 16.	R/W	0
	ACSR_BYTE_15	7-0	Audio channel status block byte 15.	R/W	0
429h	ACSR_BYTE_18	15-8	Audio channel status block byte 18.	R/W	0
	ACSR_BYTE_17	7-0	Audio channel status block byte 17.	R/W	0
42Ah	ACSR_BYTE_20	15-8	Audio channel status block byte 20.	R/W	0
	ACSR_BYTE_19	7-0	Audio channel status block byte 19.	R/W	0
42Bh	ACSR_BYTE_22	15-8	Audio channel status block byte 22.	R/W	0
	ACSR_BYTE_21	7-0	Audio channel status block byte 21.	R/W	0
42Ch	RSVD	15-8	Reserved.	R/W	0
	ACSR_BYTE_23	7-0	Audio channel status block byte 23.	R/W	0
42Dh to 43Fh	RSVD	–	Reserved.	R	0
440h	RSVD	15-9	Reserved.	R	0
	DEL1A_BYTE_1	8-1	Primary Audio group delay data for channel 1 byte 1.	R/W	0
	EBIT1A	0	Primary Audio group delay data for channel 1. HIGH = indicates delay specified at DEL1A_BYTE_1 is valid. See SMPTE Standard 272M for additional information.	R/W	0
441h	RSVD	15-9	Reserved.	R	0
	DEL1A_BYTE_2	8-0	Primary Audio group delay data for channel 1 byte 2.	R/W	0
442h	RSVD	15-9	Reserved.	R	0
	DEL1A_BYTE_3	8-0	Primary Audio group delay data for channel 1 byte 3.	R/W	0
443h	RSVD	15-9	Reserved.	R	0
	DEL2A_BYTE_1	8-1	Primary Audio group delay data for channel 2 byte 1.	R/W	0
	EBIT2A	0	Primary Audio group delay data valid flag for channel 2.	R/W	0

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
444h	RSVD	15-9	Reserved.	R	0
	DEL2A_BYTE_2	8-0	Primary Audio group delay data for channel 2 byte 2.	R/W	0
445h	RSVD	15-9	Reserved.	R	0
	DEL2A_BYTE_3	8-0	Primary Audio group delay data for channel 2 byte 3.	R/W	0
446h	RSVD	15-9	Reserved.	R	0
	DEL3A_BYTE_1	8-1	Primary Audio group delay data for channel 3 byte 1.	R/W	0
	EBIT3A	0	Primary Audio group delay data valid flag for channel 3.	R/W	0
447h	RSVD	15-9	Reserved.	R	0
	DEL3A_BYTE_2	8-0	Primary Audio group delay data for channel 3 byte 2.	R/W	0
448h	RSVD	15-9	Reserved.	R	0
	DEL3A_BYTE_3	8-0	Primary Audio group delay data for channel 3 byte 3.	R/W	0
449h	RSVD	15-9	Reserved.	R	0
	DEL4A_BYTE_1	8-1	Primary Audio group delay data for channel 4 byte 1.	R/W	0
	EBIT4A	0	Primary Audio group delay data valid flag for channel 4.	R/W	0
44Ah	RSVD	15-9	Reserved.	R	0
	DEL4A_BYTE_2	8-0	Primary Audio group delay data for channel 4 byte 2.	R/W	0
44Bh	RSVD	15-9	Reserved.	R	0
	DEL4A_BYTE_3	8-0	Primary Audio group delay data for channel 4 byte 3.	R/W	0
44Ch	RSVD	15-9	Reserved.	R	0
	DEL1B_BYTE_1	8-1	Secondary Audio group delay data for channel 1 byte 1.	R/W	0
	EBIT1B	0	Secondary Audio group delay data valid flag for channel 1.	R/W	0
44Dh	RSVD	15-9	Reserved.	R	0
	DEL1B_BYTE_2	8-0	Secondary Audio group delay data for channel 1 byte 2.	R/W	0
44Eh	RSVD	15-9	Reserved.	R	0
	DEL1B_BYTE_3	8-0	Secondary Audio group delay data for channel 1 byte 3.	R/W	0

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
44Fh	RSVD	15-9	Reserved.	R	0
	DEL2B_BYTE_1	8-1	Secondary Audio group delay data for channel 2 byte 1.	R/W	0
	EBIT2B	0	Secondary Audio group delay data valid flag for channel 2.	R/W	0
450h	RSVD	15-9	Reserved.	R	0
	DEL2B_BYTE_2	8-0	Secondary Audio group delay data for channel 2 byte 2.	R/W	0
451h	RSVD	15-9	Reserved.	R	0
	DEL2B_BYTE_3	8-0	Secondary Audio group delay data for channel 2 byte 3.	R/W	0
452h	RSVD	15-9	Reserved.	R	0
	DEL3B_BYTE_1	8-1	Secondary Audio group delay data for channel 3 byte 1.	R/W	0
	EBIT3B	0	Secondary Audio group delay data valid flag for channel 3.	R/W	0
453h	RSVD	15-9	Reserved.	R	0
	DEL3B_BYTE_2	8-0	Secondary Audio group delay data for channel 3 byte 2.	R/W	0
454h	RSVD	15-9	Reserved.	R	0
	DEL3B_BYTE_3	8-0	Secondary Audio group delay data for channel 3 byte 3.	R/W	0
455h	RSVD	15-9	Reserved.	R	0
	DEL4B_BYTE_1	8-1	Secondary Audio group delay data for channel 4 byte 1.	R/W	0
	EBIT4B	0	Secondary Audio group delay data valid flag for channel 4.	R/W	0
456h	RSVD	15-9	Reserved.	R	0
	DEL4B_BYTE_2	8-0	Secondary Audio group delay data for channel 4 byte 2.	R/W	0
457h	RSVD	15-9	Reserved.	R	0
	DEL4B_BYTE_3	8-0	Secondary Audio group delay data for channel 4 byte 3.	R/W	0

4.17 HD Audio Core Registers

Table 4-31: HD Audio Core Configuration and Status Registers

Address	Register Name	Bit	Description	R/W	Default
800h	CTR_AGR	15	Selects replacement of audio control packets. HIGH = Replace all audio control packets. LOW = Do not replace audio control packets.	R/W	0
	AGR	14	Selects Audio Group Replacement operating mode.	R/W	0
	ONE_AGR	13	Specifies the replacement of just the primary group. HIGH = Replace only the primary group. LOW = Replace both the primary and secondary groups.	R/W	0
	CTRB_ON	12	Specifies the embedding of the secondary group audio control packets. Active HIGH.	R/W	1
	ASXB	11	Secondary Group asynchronous mode. Active HIGH.	R/W	0
	AFNB_AUTO	10	Enables Secondary group audio frame number generation. Active HIGH.	R/W	1
	CTRA_ON	9	Specifies the embedding of primary group audio control packets. Active HIGH.	R/W	1
	ASXA	8	Primary Group asynchronous mode.	R/W	0
	AFNA_AUTO	7	Enables Primary group audio frame number generation.	R/W	1
	ANF_OFS	6-4	Offset to add to generated Audio Frame Number. Must be in the range of 0 to 4.	R/W	0
	IDB	3-2	Specifies the Secondary audio group to embed. 00 = Audio group #1 01 = Audio group #2 10 = Audio group #3 11 = Audio group #4	R/W	1
	IDA	1-0	Specifies the Primary audio group to embed. 00 = Audio group #1 01 = Audio group #2 10 = Audio group #3 11 = Audio group #4	R/W	0
801h	RSVD	15-0	Reserved.	R	0
802h	RSVD	15-1	Reserved.	R	0
	ACS_REGEN	0	Specifies that Audio Channel Status of all channels should be replaced with ACSR[183:0] field. HIGH = Replace Channel Status of all channels. LOW = Do not replace Channel Status.	R/W	0

Table 4-31: HD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
803h	RSVD	15-14	Reserved.	R	0
	AES_ERRD	13	Stereo Pair D audio input parity error when using AES format. Automatically cleared when read.	R	0
	AES_ERRC	12	Stereo Pair C audio input parity error when using AES format. Automatically cleared when read.	R	0
	AES_ERRB	11	Stereo Pair B audio input parity error when using AES format. Automatically cleared when read.	R	0
	AES_ERRA	10	Stereo Pair A audio input parity error when using AES format. Automatically cleared when read.	R	0
	ACPG4_DET	9	Set while Group 4 audio control packets are detected.	R	0
	ACPG3_DET	8	Set while Group 3 audio control packets are detected.	R	0
	ACPG2_DET	7	Set while Group 2 audio control packets are detected.	R	0
	ACPG1_DET	6	Set while Group 1 audio control packets are detected.	R	0
	ADPG4_DET	5	Set while Group 4 audio data packets are detected.	R	0
	ADPG3_DET	4	Set while Group 3 audio data packets are detected.	R	0
	ADPG2_DET	3	Set while Group 2 audio data packets are detected.	R	0
	ADPG1_DET	2	Set while Group 1 audio data packets are detected.	R	0
	ACS_APPLY_WAITB	1	Set while the GV7600 is waiting for a status boundary in the Secondary group before applying the ACSR[183:0] data to that group.	R	0
	ACS_APPLY_WAITA	0	ACS_APPLY_WAITA: Set while the multiplexer is waiting for a status boundary in Primary group before applying the ACSR[183:0] data.	R	0
804h	RSVD	15-0	Reserved.	R	0
805h	RSVD	15-1	Reserved.	R	0
	EN_CASCADE	0	If HIGH, puts the GV7600 into cascade mode. This bit is only effective if the AGR bit = LOW.	R/W	0
806h to 809h	RSVD	-	Reserved.	R	0

Table 4-31: HD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
80Ah	AMD	15-14	Audio input format selector for Stereo Pair D input channels 7 and 8. 00 = AES/EBU or S/PDIF 01 = Serial Left Justified, MSB First 10 = Serial Right Justified, MSB First 11 = I^2S (Default)	R/W	3
	AMC	13-12	Audio input format selector for Stereo Pair C input channels 5 and 6. (See above for decoding.)	R/W	3
	AMB	11-10	Audio input format selector for Stereo Pair B input channels 3 and 4. (See above for decoding.)	R/W	3
	AMA	9-8	Audio input format selector for Stereo Pair A input channels 1 and 2. (See above for decoding.)	R/W	3
	MUTE8	7	Audio input channel 8 mute enable.	R/W	0
	MUTE7	6	Audio input channel 7 mute enable.	R/W	0
	MUTE6	5	Audio input channel 6 mute enable.	R/W	0
	MUTE5	4	Audio input channel 5 mute enable.	R/W	0
	MUTE4	3	Audio input channel 4 mute enable.	R/W	0
	MUTE3	2	Audio input channel 3 mute enable.	R/W	0
	MUTE2	1	Audio input channel 2 mute enable.	R/W	0
	MUTE1	0	Audio input channel 1 mute enable.	R/W	0
80Bh	RSVD	15	Reserved.	R	0
	GPA_WCLK_SRC	14-12	Primary Audio group word clock source selector.	R/W	0
	GPA_CH4_SRC	11-9	Primary Audio group channel 4 source selector.	R/W	3
	GPA_CH3_SRC	8-6	Primary Audio group channel 3 source selector.	R/W	2
	GPA_CH2_SRC	5-3	Primary Audio group channel 2 source selector.	R/W	1
	GPA_CH1_SRC	2-0	Primary Audio group channel 1 source selector.	R/W	0
80Ch	RSVD	15	Reserved.	R	0
	GPB_WCLK_SRC	14-12	Secondary Audio group word clock source selector.	R/W	4
	GPB_CH4_SRC	11-9	Secondary Audio group channel 4 source selector.	R/W	7
	GPB_CH3_SRC	8-6	Secondary Audio group channel 3 source selector.	R/W	6
	GPB_CH2_SRC	5-3	Secondary Audio group channel 2 source selector.	R/W	5
	GPB_CH1_SRC	2-0	Secondary Audio group channel 1 source selector.	R/W	4

Table 4-31: HD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
80Dh	RSVD	15	Reserved.	R	0
	EN_NO_VIDEO	14	Asserts AUDIO_INT when the video format is unknown. i.e. when NO_VIDEO register bit is set.	R/W	0
	RSVD	13-12	Reserved.	R/W	0
80Dh	EN_AES_ERRD	11	Asserts AUDIO_INT when the AES_ERRD flag is set.	R/W	0
	EN_AES_ERRC	10	Asserts AUDIO_INT when the AES_ERRC flag is set.	R/W	0
	EN_AES_ERRB	9	Asserts AUDIO_INT when the AES_ERRB flag is set.	R/W	0
	EN_AES_ERRA	8	Asserts AUDIO_INT when the AES_ERRA flag is set.	R/W	0
	EN_ACPG4_DET	7	Asserts AUDIO_INT when the ACPG4_DET flag is set.	R/W	0
	EN_ACPG3_DET	6	Asserts AUDIO_INT when the ACPG3_DET flag is set.	R/W	0
	EN_ACPG2_DET	5	Asserts AUDIO_INT when the ACPG2_DET flag is set.	R/W	0
	EN_ACPG1_DET	4	Asserts AUDIO_INT when the ACPG1_DET flag is set.	R/W	0
	EN_ADPG4_DET	3	Asserts AUDIO_INT when the ADPG4_DET flag is set.	R/W	0
	EN_ADPG3_DET	2	Asserts AUDIO_INT when the ADPG3_DET flag is set.	R/W	0
	EN_ADPG2_DET	1	Asserts AUDIO_INT when the ADPG2_DET flag is set.	R/W	0
	EN_ADPG1_DET	0	Asserts AUDIO_INT when the ADPG1_DET flag is set.	R/W	0

Table 4-31: HD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
80Eh	RSVD	15-13	Reserved.	R	0
	MUTE_ALL	12	Mutes all input audio channels.	R/W	0
	LSB_FIRSTD	11	Causes the fourth stereo pair serial input formats to use LSB first.	R/W	0
	LSB_FIRSTC	10	Causes the third stereo pair serial input formats to use LSB first.	R/W	0
	LSB_FIRSTB	9	Causes the second stereo pair serial input formats to use LSB first.	R/W	0
	LSB_FIRSTA	8	Causes the first stereo pair serial input formats to use LSB first.	R/W	0
	ACT8	7	Specifies embedding of secondary audio group channel 8.	R/W	1
	ACT7	6	Specifies embedding of secondary audio group channel 7.	R/W	1
	ACT6	5	Specifies embedding of secondary audio group channel 6.	R/W	1
	ACT5	4	Specifies embedding of secondary audio group channel 5.	R/W	1
	ACT4	3	Specifies embedding of secondary audio group channel 4.	R/W	1
	ACT3	2	Specifies embedding of secondary audio group channel 3.	R/W	1
	ACT2	1	Specifies embedding of secondary audio group channel 2.	R/W	1
	ACT1	0	Specifies embedding of secondary audio group channel 1.	R/W	1
80Fh	RSVD	15-1	Reserved.	R	0
	XPOINT_ERROR	0	Set when the crosspoint switch is configured to put the same audio channel in both Primary and Secondary Groups.	R	0
810h to 81Fh	RSVD	–	Reserved.	R	0
820h	RSVD	15-8	Reserved.	R	0
	ACSR_BYTE_1	7-0	Audio channel status block byte 1.	R/W	133
821h	RSVD	15-8	Reserved.	R	0
	ACSR_BYTE_2	7-0	Audio channel status block byte 2.	R/W	8
822h	ACSR_BYTE_4	15-8	Audio channel status block byte 4.	R/W	0
	ACSR_BYTE_3	7-0	Audio channel status block byte 3.	R/W	44

Table 4-31: HD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
823h	ACSR_BYTE_6	15-8	Audio channel status block byte 6.	R/W	0
	ACSR_BYTE_5	7-0	Audio channel status block byte 5.	R/W	0
824h	ACSR_BYTE_8	15-8	Audio channel status block byte 8.	R/W	0
	ACSR_BYTE_7	7-0	Audio channel status block byte 7.	R/W	0
825h	ACSR_BYTE_10	15-8	Audio channel status block byte 10.	R/W	0
	ACSR_BYTE_9	7-0	Audio channel status block byte 9.	R/W	0
826h	ACSR_BYTE_12	15-8	Audio channel status block byte 12.	R/W	0
	ACSR_BYTE_11	7-0	Audio channel status block byte 11.	R/W	0
827h	ACSR_BYTE_14	15-8	Audio channel status block byte 14.	R/W	0
	ACSR_BYTE_13	7-0	Audio channel status block byte 13.	R/W	0
828h	ACSR_BYTE_16	15-8	Audio channel status block byte 16.	R/W	0
	ACSR_BYTE_15	7-0	Audio channel status block byte 15.	R/W	0
829h	ACSR_BYTE_18	15-8	Audio channel status block byte 18.	R/W	0
	ACSR_BYTE_17	7-0	Audio channel status block byte 17.	R/W	0
82Ah	ACSR_BYTE_20	15-8	Audio channel status block byte 20.	R/W	0
	ACSR_BYTE_19	7-0	Audio channel status block byte 19.	R/W	0
82Bh	ACSR_BYTE_22	15-8	Audio channel status block byte 22.	R/W	0
	ACSR_BYTE_21	7-0	Audio channel status block byte 21.	R/W	0
82Ch	RSVD	15-8	Reserved.	R	0
	ACSR_BYTE_23	7-0	Audio channel status block byte 23.	R/W	0
82Dh to 83Fh	RSVD	–	Reserved.	R	0
840h	RSVD	15-9	Reserved.	R	0
	DEL1_2A_BYTE_1	8-1	Primary Audio group delay data for channel 1 & 2.	R/W	0
	EBIT1_2A	0	Primary Audio group delay data valid flag for channel 1 & 2.	R/W	0
841h	RSVD	15-9	Reserved.	R	0
	DEL1_2A_BYTE_2	8-0	Primary Audio group delay data for channel 1 & 2.	R/W	0
842h	RSVD	15-9	Reserved.	R	0
	DEL1_2A_BYTE_3	8-0	Primary Audio group delay data for channel 1 & 2.	R/W	0

Table 4-31: HD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
843h	RSVD	15-9	Reserved.	R	0
	DEL3_4A_BYTE_1	8-1	Primary Audio group delay data for channel 3 & 4.	R/W	0
	EBIT3_4A	0	Primary Audio group delay data valid flag for channel 3 & 4.	R/W	0
844h	RSVD	15-9	Reserved.	R	0
	DEL3_4A_BYTE_2	8-0	Primary Audio group delay data for channel 3 & 4.	R/W	0
845h	RSVD	15-9	Reserved.	R	0
	DEL3_4A_BYTE_3	8-0	Primary Audio group delay data for channel 3 & 4.	R/W	0
846h	RSVD	15-9	Reserved.	R	0
	DEL1_2B_BYTE_1	8-1	Secondary Audio group delay data for channel 1 & 2.	R/W	0
	EBIT1_2B	0	Secondary Audio group delay data valid flag for channel 1 & 2.	R/W	0
847h	RSVD	15-9	Reserved.	R	0
	DEL1_2B_BYTE_2	8-0	Secondary Audio group delay data for channel 1 & 2.	R/W	0
848h	RSVD	15-9	Reserved.	R	0
	DEL1_2B_BYTE_3	8-0	Secondary Audio group delay data for channel 1 & 2.	R/W	0
849h	RSVD	15-9	Reserved.	R	0
	DEL3_4B_BYTE_1	8-1	Secondary Audio group delay data for channel 3 & 4.	R/W	0
	EBIT3_4B	0	Secondary Audio group delay data for channel 3 & 4.	R/W	0
84Ah	RSVD	15-9	Reserved.	R	0
	DEL3_4B_BYTE_2	8-0	Secondary Audio group delay data for channel 3 & 4.	R/W	0
84Bh	RSVD	15-9	Reserved.	R	0
	DEL3_4B_BYTE_3	8-0	Secondary Audio group delay data for channel 3 & 4.	R/W	0

4.18 Device Power-Up

The GV7600 is designed to operate in a multi-voltage environment, therefore, any power-up sequence is allowed. The Charge Pump, Phase Detector, Core Logic, Serial Digital Output and I/O Buffers can all be powered up in any order.

4.19 Device Reset

Note: At power-up, the device must be reset to operate correctly.

In order to initialize all internal operating conditions to their default states, hold the $\overline{\text{RESET}}$ signal LOW for a minimum of t_{reset} = 1ms after all power supplies are stable. There are no requirements for power supply sequencing.

When held in reset, all device outputs are driven to a high-impedance state.

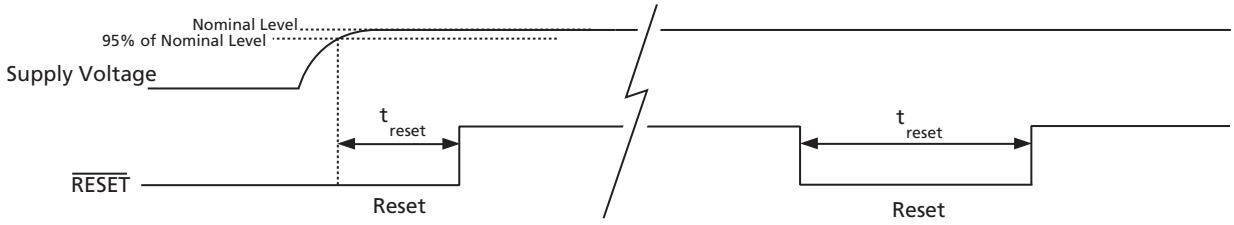


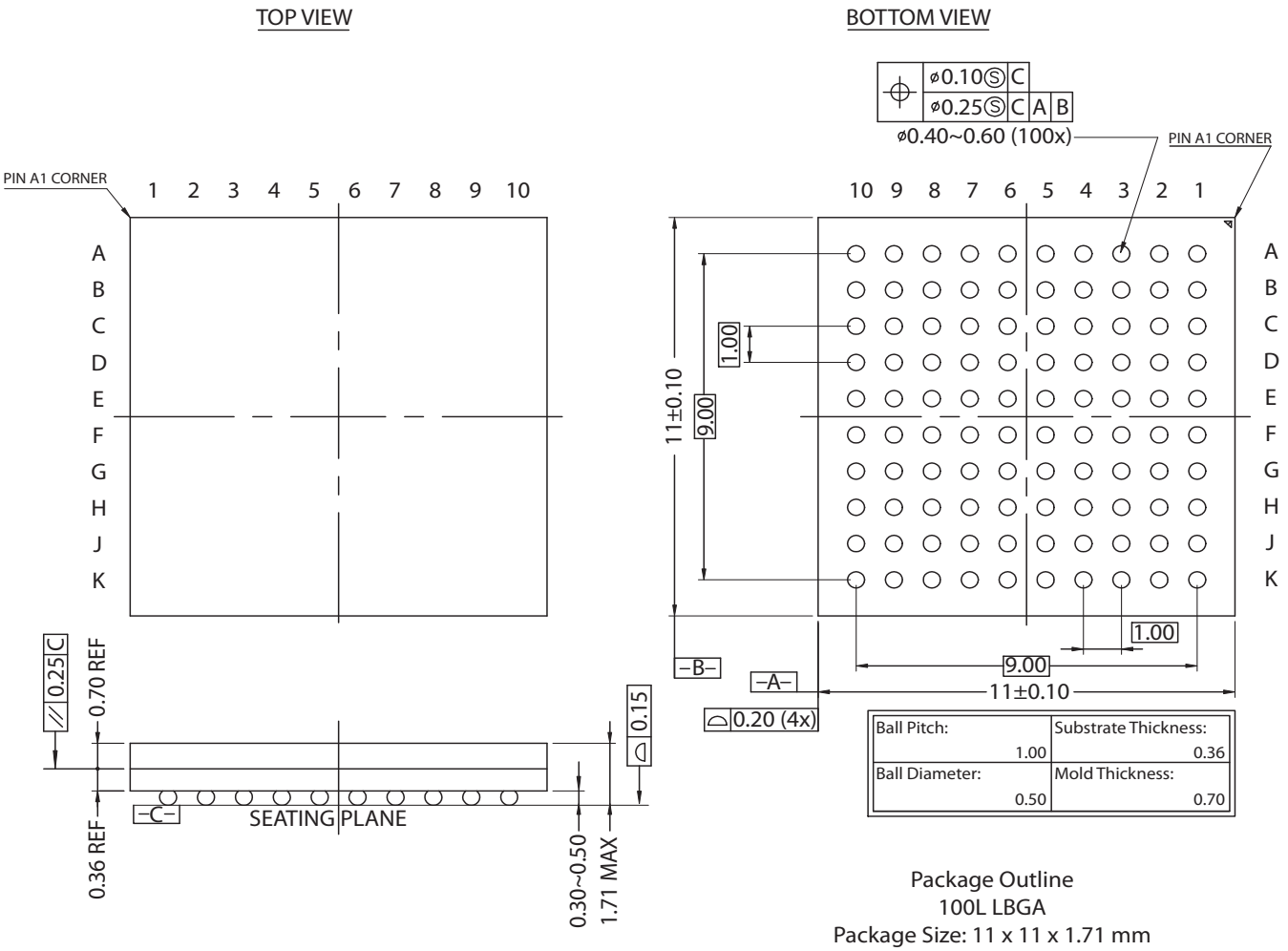
Figure 4-55: Reset Pulse

5. References & Relevant Standards

EN 50083-9	Interfaces for CATV/SMATV headends and similar professional equipment for DVG/MPEG-2 transport streams
ISO/IEC 13818-1	Generic Coding of Moving Pictures and Associated Audio Systems
ITU-R BT.1120-6	Digital interfaces for HDTV studio signals
ITU-R BT.656	Interface for digital component video signals
ITU-R BT.709	Parameter values for the HDTV standards for production and international programme exchange
SMPTE ST 272	Formatting AES Audio and Auxiliary Data into Digital Video Ancillary Data Space
SMPTE ST 291	Ancillary Data Packet and Space Formatting
SMPTE ST 296	1280 x 720 Progressive Image Sample Structure - Analog and Digital Representation and Analog Interface
SMPTE ST 299	24-Bit Digital Audio Format for SMPTE ST 292 Bit-Serial Interface
SMPTE RP165	Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television

6. Package & Ordering Information

6.1 Package Dimensions



Package Outline
100L LBGA
Package Size: 11 x 11 x 1.71 mm

* The ball diameter, ball pitch, stand-off & package thickness are different from JEDEC spec M0192 (Low profile BGA family)

Figure 6-1: GV7600 Package Dimensions

6.2 Packaging Data

Table 6-1: Packaging Data

Parameter	Value
Package Type	11mm x 11mm 100-ball LBGA
Package Drawing Reference	JEDEC M0192 (with exceptions noted in 6.1 Package Dimensions).
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	10.4°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	37.1°C/W
Junction to Board Thermal Resistance, θ_{j-b}	26.4°C/W
Psi, ψ	0.4°C/W
Pb-free and RoHS Compliant	Yes

6.3 Marking Diagram

Figure 6-2: GV7600 Marking Diagram

6.4 Solder Reflow Profiles

The GV7600 is available in a Pb-free package. It is recommended that the Pb-free package be soldered with Pb-free paste using the reflow profile shown in Figure 6-3.

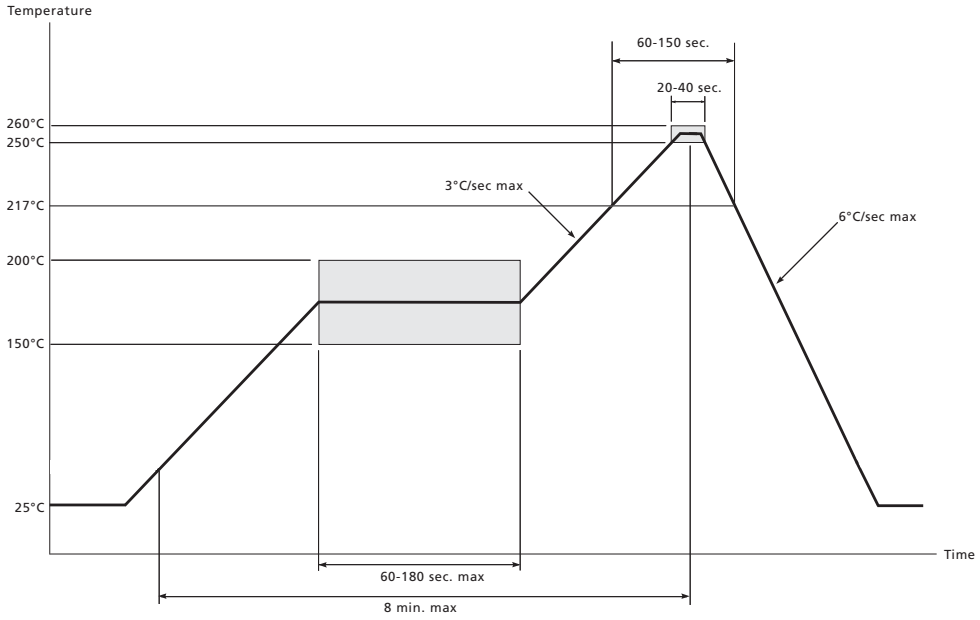


Figure 6-3: Pb-free Solder Reflow Profile

6.5 Ordering Information

Part Number	Package	Pb-free	Temperature Range
GV7600-IBE3	100-ball BGA	Yes	-20°C to 85°C

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Aviia™ is Gennum's high bandwidth, all digital, long reach A/V interface for professional and industrial applications; providing high definition video, digital audio, bi-directional control and power over a single-wire robust and cost effective interface.

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