PI74AVC+16268

12-Bit to 24-Bit Registered Bus Exchanger with 3-State Outputs

Product Features

- PI74AVC+16268 is designed for low-voltage operation, V_{CC} = 1.65V to 3.6V
- True ±24mA Balanced Drive @ 3.3V
- I_{OFF} supports partial power-down operation
- 3.6 I/O Tolerant Inputs and Outputs
- All outputs contain a patented DDC (Dynamic DriveControl) circuit that reduces noise without degrading propagation delay.
- Industrial operation: –40°C to +85°C
- Available Packages:
  – 56-pin 240 mil wide plastic TSSOP (A)
  – 56-pin 173 mil wide plastic TVSOP (K)

Product Description

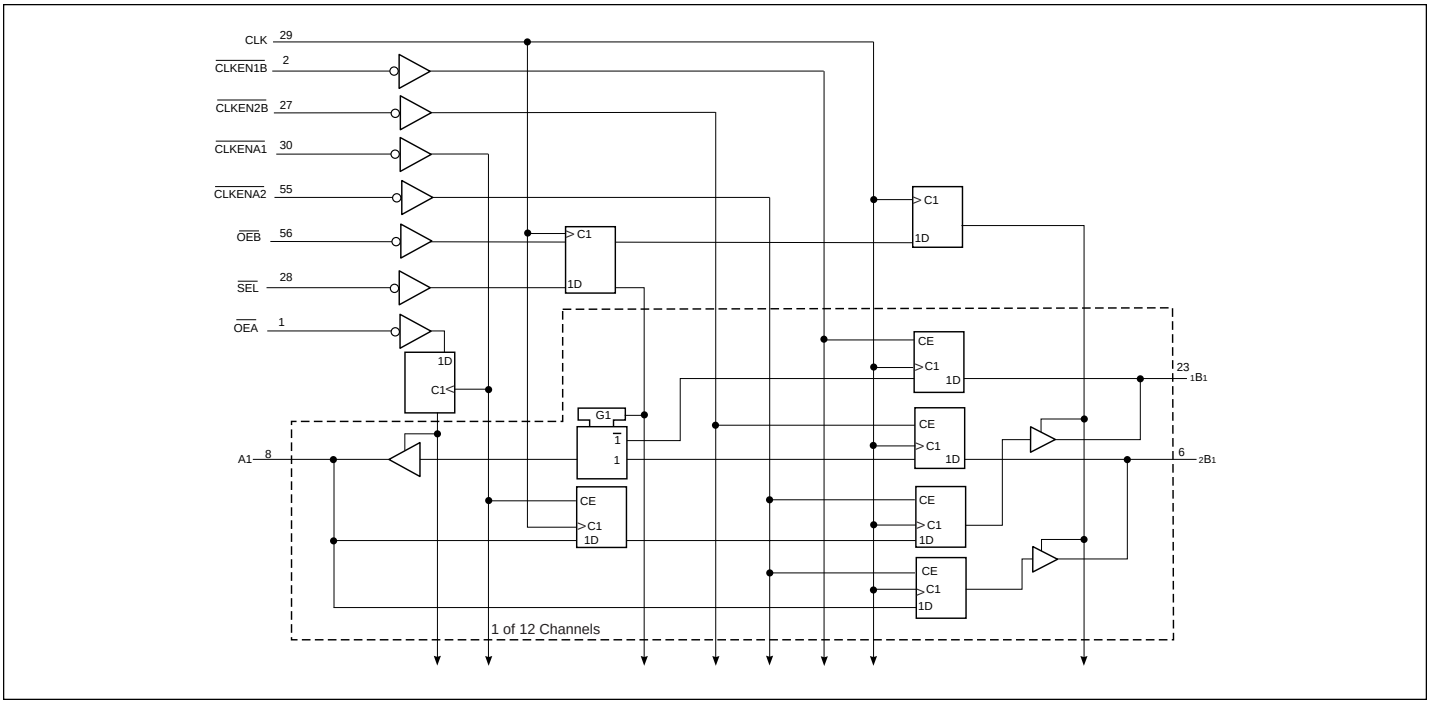
Pericom Semiconductor's PI74AVC+ series of logic circuits are produced using the Company's advanced submicron CMOS technology, achieving industry leading speed.

The PI74AVC+16268, a 12-bit to 24-bit registered bus exchanger designed for 1.65V to 3.6V V_{CC} operation, is used for applications in which data must be transferred from a narrow high-speed bus to a wide, lower frequency bus. It provides synchronous data exchange between the two ports. Data is stored in internal registers on the low-to-high transition of the clock (CLK) input when appropriate clock-enable ($\overline{CLKEN}$) inputs are low. The select ($\overline{SEL}$) line is synchronous with CLK and selects 1B or 2B input data for the A outputs.

For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path, with a single storage register in the A-to-2B path. Proper control of these inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B-port. Data flow is controlled by the active-low output enables ($\overline{OEA}$, $\overline{OEB}$). These control terminals are registered so bus direction changes are synchronous with CLK.

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible and $\overline{OE}$ should be tied to V_{CC} through a pullup resistor, the minimum value of the resistor is determined by the current-sinking capability of the driver. Because $\overline{OE}$ is being routed through a register, the active state of the outputs cannot be determined prior to the arrival of the first clock pulse.

Logic Block Diagram



Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
CLK	Clock
$\overline{SEL}$	Select (Active Low)
$\overline{CLKEN}$	Clock Enable (Active Low)
A,1B,2B	3-State Outputs
GND	Ground
V_{CC}	Power

Truth Tables(1)

Output Enable

Inputs			Outputs	
CLK	$\overline{OEA}$	$\overline{OEB}$	A	1B,2B
—	H	H	Z	Z
—	H	L	Z	Active
—	L	H	Active	Z
—	L	L	Active	Active

A to B STORAGE ($\overline{OEB}$ = L)

Inputs				Outputs	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
H	H	X	X	1B0(2)	2B0(3)
L	L	↑	L	L(2)	X
L	L	↑	H	H(2)	X
X	L	↑	L	X	L
X	L	↑	H	X	H

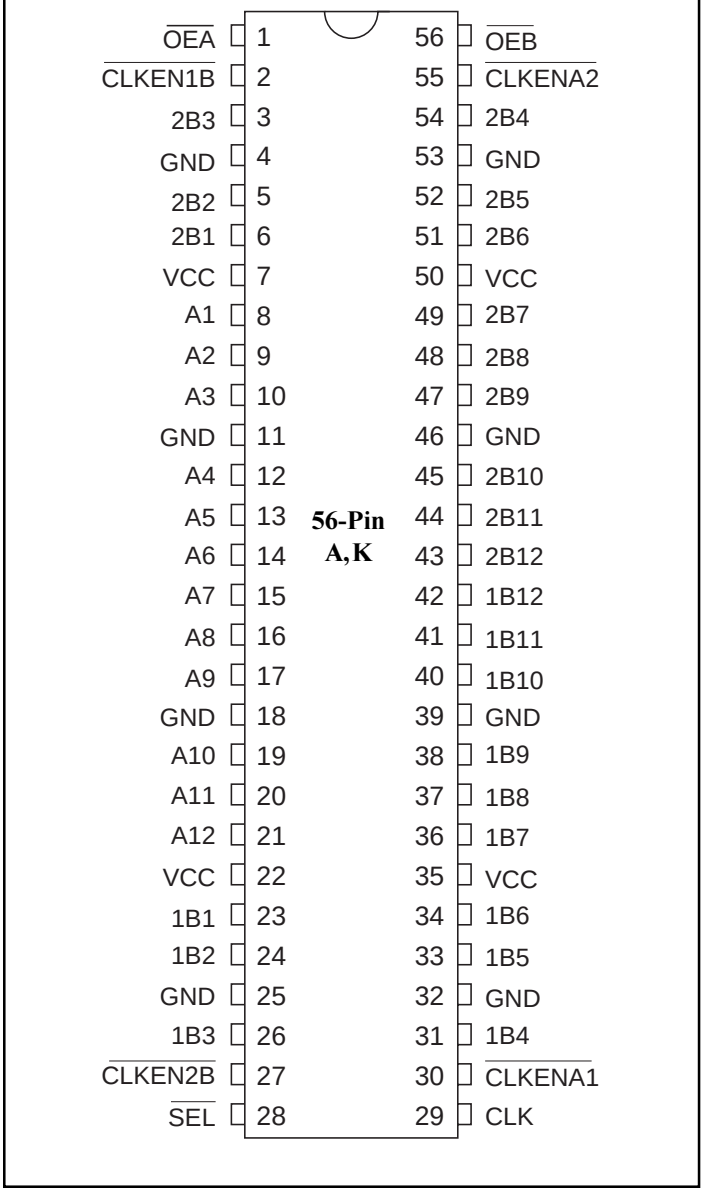
B to A STORAGE ($\overline{OEA}$ = L)

Inputs						Outputs A
$\overline{CLKEN1B}$	$\overline{CLKEN2B}$	CLK	$\overline{SEL}$	1B	2B	
H	X	X	H	X	X	A0(3)
X	H	X	L	X	X	A0(3)
L	X	↑	H	L	X	L
L	X	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

Notes:

1. H = High Signal Level, L = Low Signal Level, X = Irrelevant, Z = High Impedance, ↑ = Transition, Low to High
2. Two CLK edges are needed to propagate data
3. Output level before indicated steady state input conditions were established.

Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired.
For user guidelines, not tested.)

Supply voltage range, V_{CC} ..... –0.5V to +4.6V
Input voltage range, V_I ..... –0.5V to +4.6V
Voltage range applied to any output in the high-impedance or power-off state, V_O[1] ..... –0.5V to +4.6V
Voltage range applied to any output in the high or low state, V_O[1,2] ..... –0.5V to V_{CC} +0.5V
Input clamp current, I_{IK} (V_I <0) ..... –50mA
Output clamp current, I_{OK} (V_O <0) ..... –50mA
Continuous output current, I_O ..... ±50mA
Continuous current through each V_{CC} or GND ..... ±100mA
Package thermal impedance, θ_{JA}[3]: package A ..... 64°C/W
package K ..... 48°C/W
Storage Temperature range, T_{stg} ..... –65°C to 150°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Notes:
1. Input & output negative-voltage ratings may be exceeded if the input and output curent rating are observed.
2. Output positive-voltage rating may be exceeded up to 4.6V maximum if theoutput current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD51.

Recommended Operating Conditions[1]

		Min.	Max.	Units
V_{CC} Supply Voltage	Operating	1.65	3.6	V
	Data retention only	1.2		
V_{IH} High-level Input Voltage	V_{CC} = 1.2V	V_{CC}		
	V_{CC} = 1.65V to 1.95V	0.65 x V_{CC}		
	V_{CC} = 2.3V to 2.7V	1.7		
	V_{CC} = 3V to 3.6V	2		
V_{IL} Low-level Input Voltage	V_{CC} = 1.2V		GND	
	V_{CC} = 1.65V to 1.95V		0.35 x V_{CC}	
	V_{CC} = 2.3V to 2.7V		0.7	
	V_{CC} = 3V to 3.6V		0.8	
V_I Input Voltage		0	3.6	
V_O Output Voltage	Active State	0	V_{CC}	
	3-State	0	3.6	
I_{OH} High-level output current	V_{CC} = 1.65V to 1.95V		– 6	mA
	V_{CC} = 2.3V to 2.7V		– 12	
	V_{CC} = 3V to 3.6V		– 24	
I_{OL} Low-level output current	V_{CC} = 1.65V to 1.95V		6	
	V_{CC} = 2.3V to 2.7V		12	
	V_{CC} = 3V to 3.6V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate	V_{CC} = 1.65V to 3.6V		5	ns/V
T_A Operating free-air temperature		–40	85	°C

Notes:
1. All unused inputs must be held at V_{CC} or GND to ensure proper device operation.

DC Electrical Characteristics (Over the Operating Range, $T_A = –40°C$ +85°C)

Parameters		Test Conditions[1]	V_{CC}	Min.	Max.	Units
V_{OH}		I_{OH} = –100µA	1.65V to 3.6V	V_{CC} –0.2V		V
		I_{OH} = –6mA V_{IH} = 1.07V	1.65V	1.2		
		I_{OH} = –12mA V_{IH} = 1.7V	2.3V	1.75		
		I_{OH} = –24mA V_{IH} = 2V	3V	2.0		
V_{OL}		I_{OL} = 100µA	1.65V to 3.6V		0.2	
		I_{OL} = 6mA V_{IH} = 0.57V	1.65V		0.45	
		I_{OL} = 12mA V_{IH} = 0.7V	2.3V		0.55	
		I_{OL} = 24mA V_{IH} = 0.8V	3V		0.8	
I_I	Control Inputs	$V_I = V_{CC}$ or GND	3.6V		±2.5	µA
I_{OFF}		V_I or V_O = 3.6V	0		±10	
I_{OZ}		$V_I = V_{CC}$ or GND	3.6V		±10	
I_{CC}		$V_O = V_{CC}$ or GND I_O = 0	3.6V		40	
C_I	Control Inputs	$V_I = V_{CC}$ or GND	2.5V		4	pF
			3.3V		4	
	Data Inputs		2.5V		6	
			3.3V		6	
C_O	Outputs	$V_O = V_{CC}$ or GND	2.5V		8	
			3.3V		8	

Note:
1. Typical values are measured at $T_A = 25°C$.

Timing Requirements (Over Operating Range)

Parameters	Description		V_{CC} = 1.2V		V_{CC} = 1.5V ±0.1V		V_{CC} = 1.8V ±0.15V		V_{CC} = 2.5V ±0.2V		V_{CC} = 3.3V ±0.3V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLOCK}	Clock frequency							150		180		180	MHz
t_W	Pulse duration, CLK high or low						3		3		3		ns
t_{SU}	Setup time	A data before CLK↑	2.2		2.2		2.0		1.5		1.5		
		B data before CLK↑	1.6		1.5		1.5		1.0		0.8		
		$\overline{SEL}$ before CLK↑	2.0		1.8		1.5		1.3		1.1		
		$\overline{CLKENA1}$ or $\overline{CLKENA2}$ before CLK↑	3.2		2.2		2.0		1.8		1.7		
		$\overline{CLKENB1}$ or $\overline{CLKENB2}$ before CLK↑	3.2		2.4		2.0		1.8		1.7		
		$\overline{OE}$ before CLK↑	3.2		2.5		2.2		2.2		2.0		
t_H	Hold time	A data after CLK↑	0.5		0.5		0.2		0.2		0.1		
		B data after CLK↑	1.0		1.0		1.0		1.0		1.0		
		$\overline{SEL}$ after CLK↑	1.4		1.4		1.0		1.0		0.8		
		$\overline{CLKENA1}$ or $\overline{CLKENA2}$ after CLK↑	0		0		0.2		0.6		0.6		
		CLKENB1 or CLKENB2 after CLK↑	0		0		0.1		0.6		0.6		
		$\overline{OE}$ after CLK↑	0		0.2		0.2		0.5		0.5		

Note:
1. Unused control inputs must be held HIGH or LOW to prevent them from floating.

Switching Characteristics (Over Operating Range)

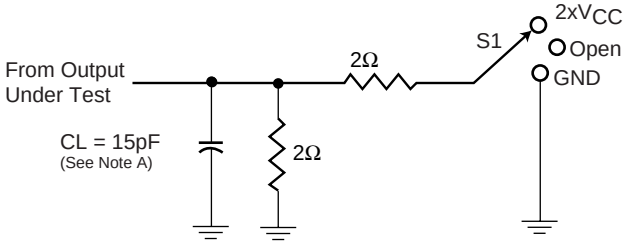
Parameter	From (Input)	To (Output)	V_{CC} = 1.2V	V_{CC} = 1.5V ±0.1V		V_{CC} = 1.8V ±0.15V		V_{CC} = 2.5V ±0.2V		V_{CC} = 3.3V ±0.3V		Units
			Typical	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{max}						150		180		180		MHz
t_{pd}	CLK	B	8.1		5.0	2.0	4.8	1.8	4.0	1.3	3.1	ns
		A(1B)	9.0		5.5	2.1	5.0	1.7	4.2	1.2	3.4	
		B(2B)	8.0		5.5	2.1	5.0	1.8	4.3	1.3	3.4	
		A(SEL)	9.3		6.5	2.5	5.4	2.4	4.3	1.7	3.6	
t_{en}	CLK	B	9.3		6.4	2.8	5.8	2.6	4.4	1.8	3.8	
t_{dis}		B	9.0		7.0	3.0	6.0	2.5	3.8	1.8	3.8	
t_{en}		A	9.0		6.5	2.1	5.5	1.8	4.2	1.3	3.6	
t_{dis}		A	8.8		6.3	2.3	5.5	2.1	3.5	1.5	3.8	

Notes:
1. Unused control inputs must be held HIGH or LOW to prevent them from floating.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Operating Characteristics, T_A= 25°C

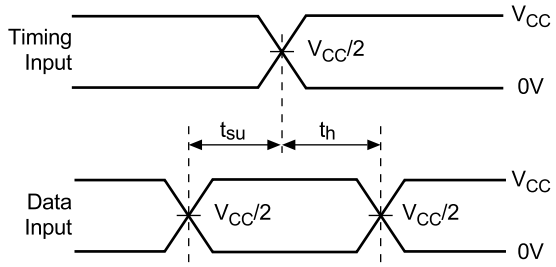
Parameters		Test Conditions	V_{CC} = 1.8V ±0.15V	V_{CC} = 2.5V ±0.2V	V_{CC} = 3.3V ±0.3V	Units
			Typical	Typical	Typical	
Cpd Power Dissipation Capacitance	Outputs Enabled	C_L = 0pF, f = 10 MHz	60	65	76	pF
	Outputs Disabled		40	45	55	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 1.2V and 1.5V ±0.1V

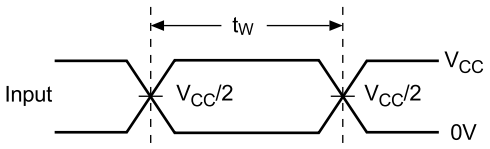


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

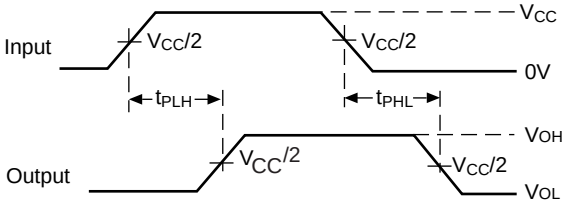
Load Circuit



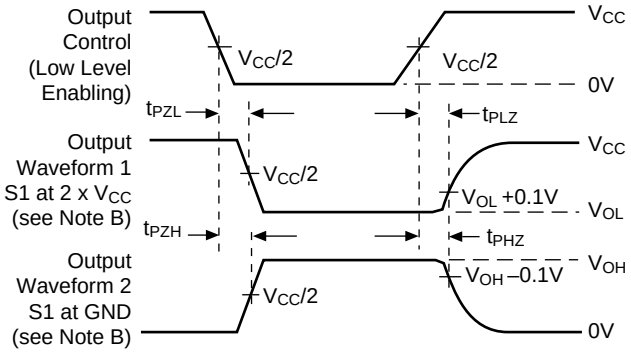
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



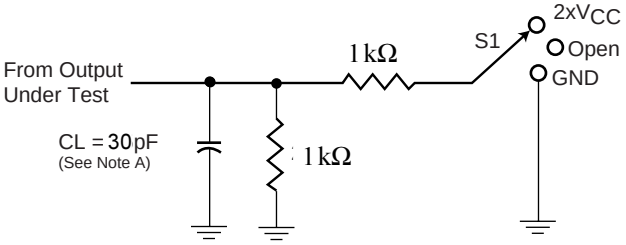
Voltage Waveforms
Enable and Disable Times

Figure 1. Load Circuit and Voltage Waveforms

Notes:

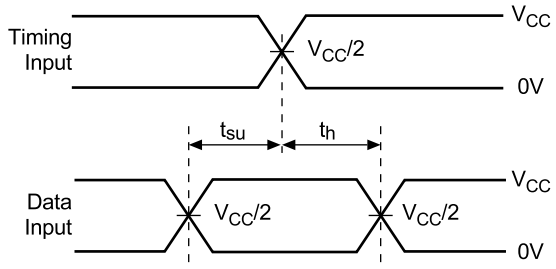
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 1.8V ±0.15V

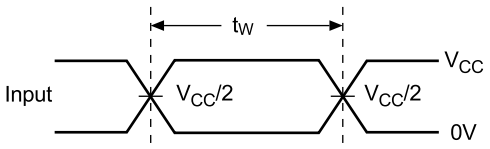


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

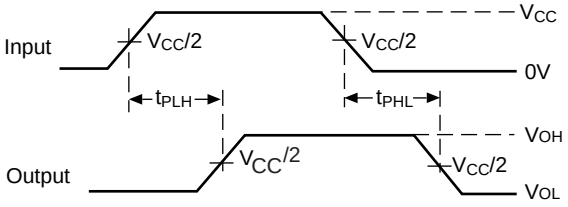
Load Circuit



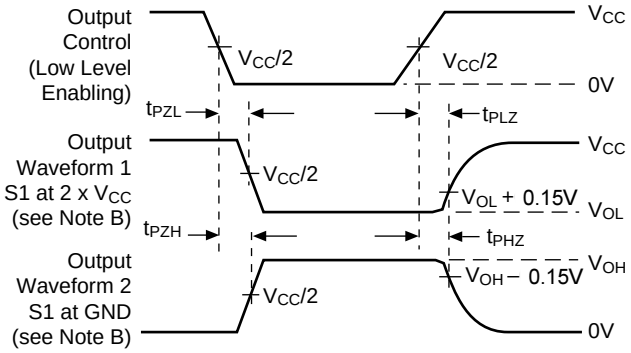
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



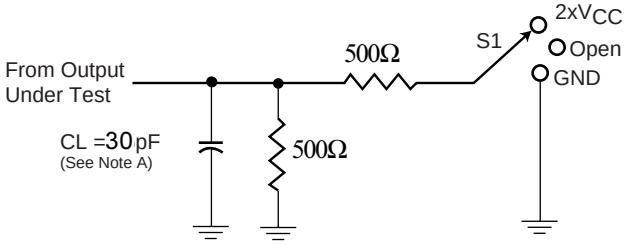
Voltage Waveforms
Enable and Disable Times

Figure 2. Load Circuit and Voltage Waveforms

Notes:

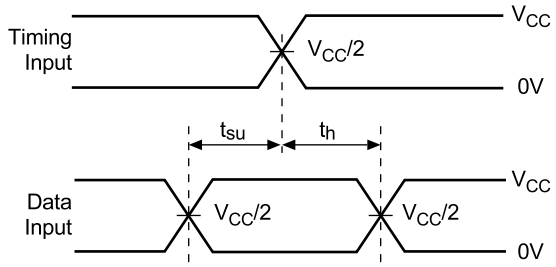
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5V ±0.2V

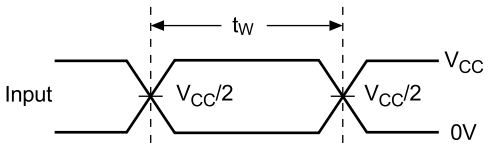


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

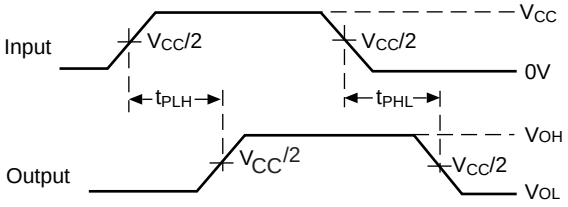
Load Circuit



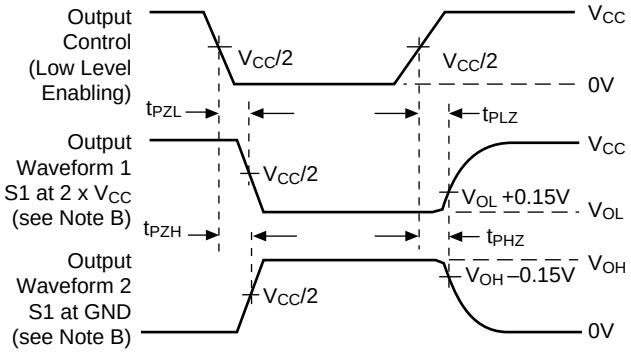
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

Figure 3. Load Circuit and Voltage Waveforms

Notes:

A. C_L includes probe and jig capacitance.
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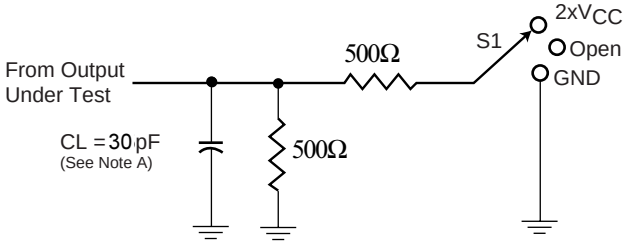
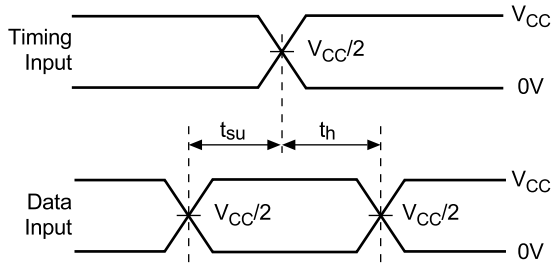
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 3.3V ±0.3V

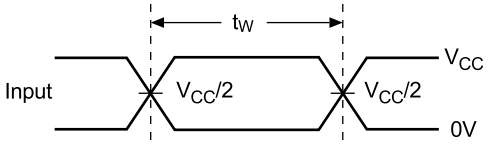


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

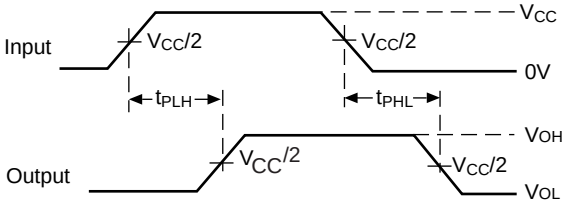
Load Circuit



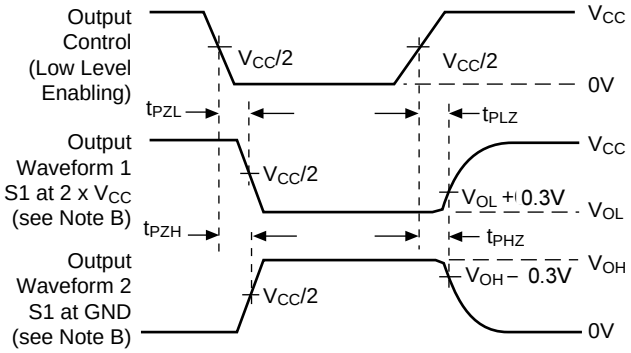
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



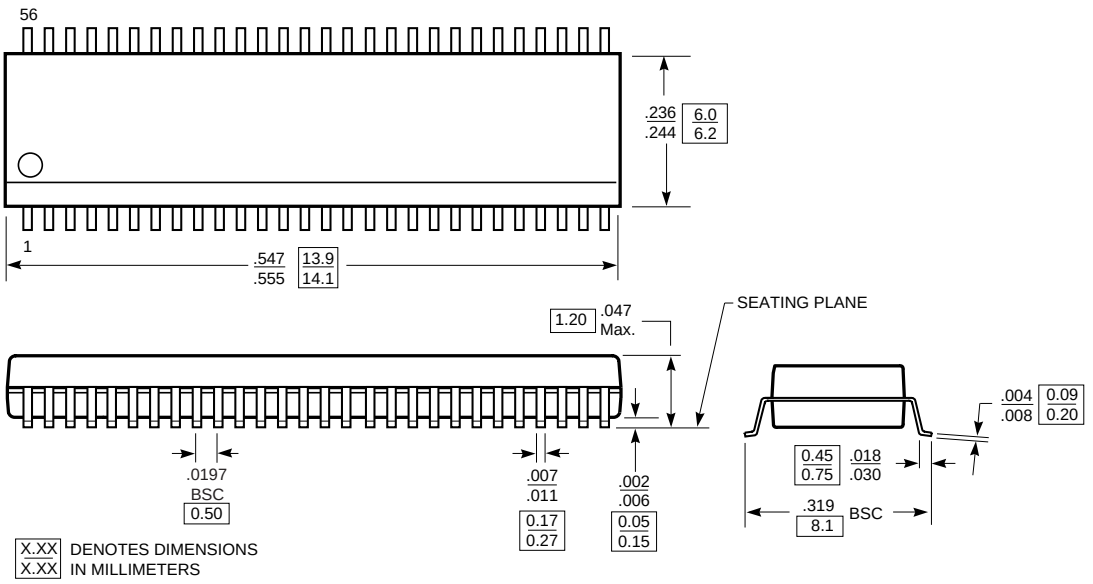
Voltage Waveforms
Enable and Disable Times

Figure 4. Load Circuit and Voltage Waveforms

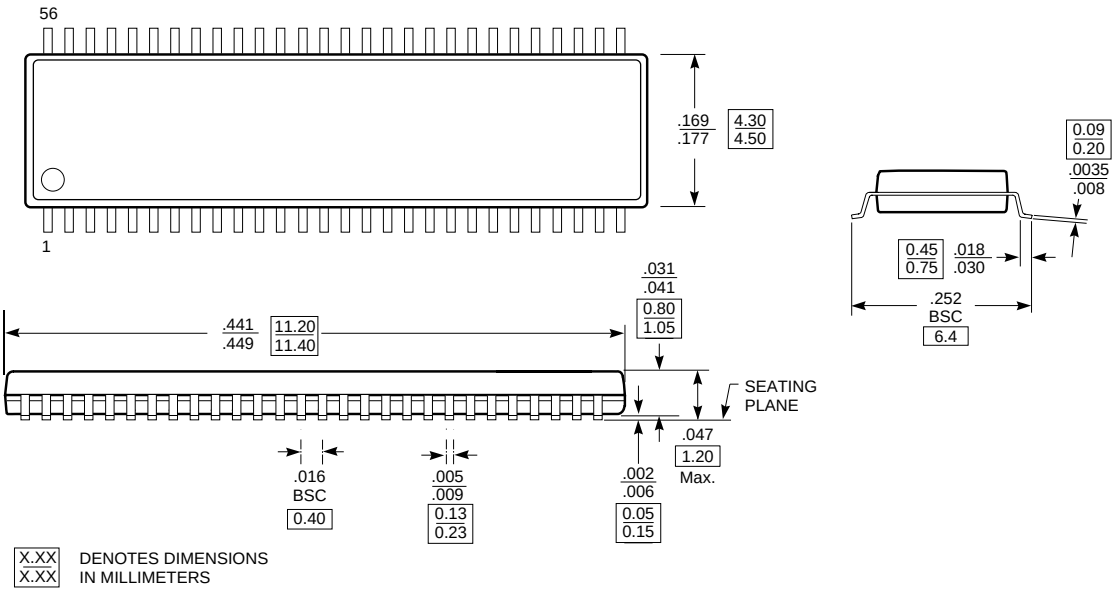
Notes:

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}

56-pin TSSOP (A) Package



56-pin TVSOP (K) Package



Ordering Information

Ordering Data	Description
PI74AVC+16268A	56-pin, 240 mil wide plastic TSSOP
PI74AVC+16268K	56-pin, 173 mil wide plastic TVSOP